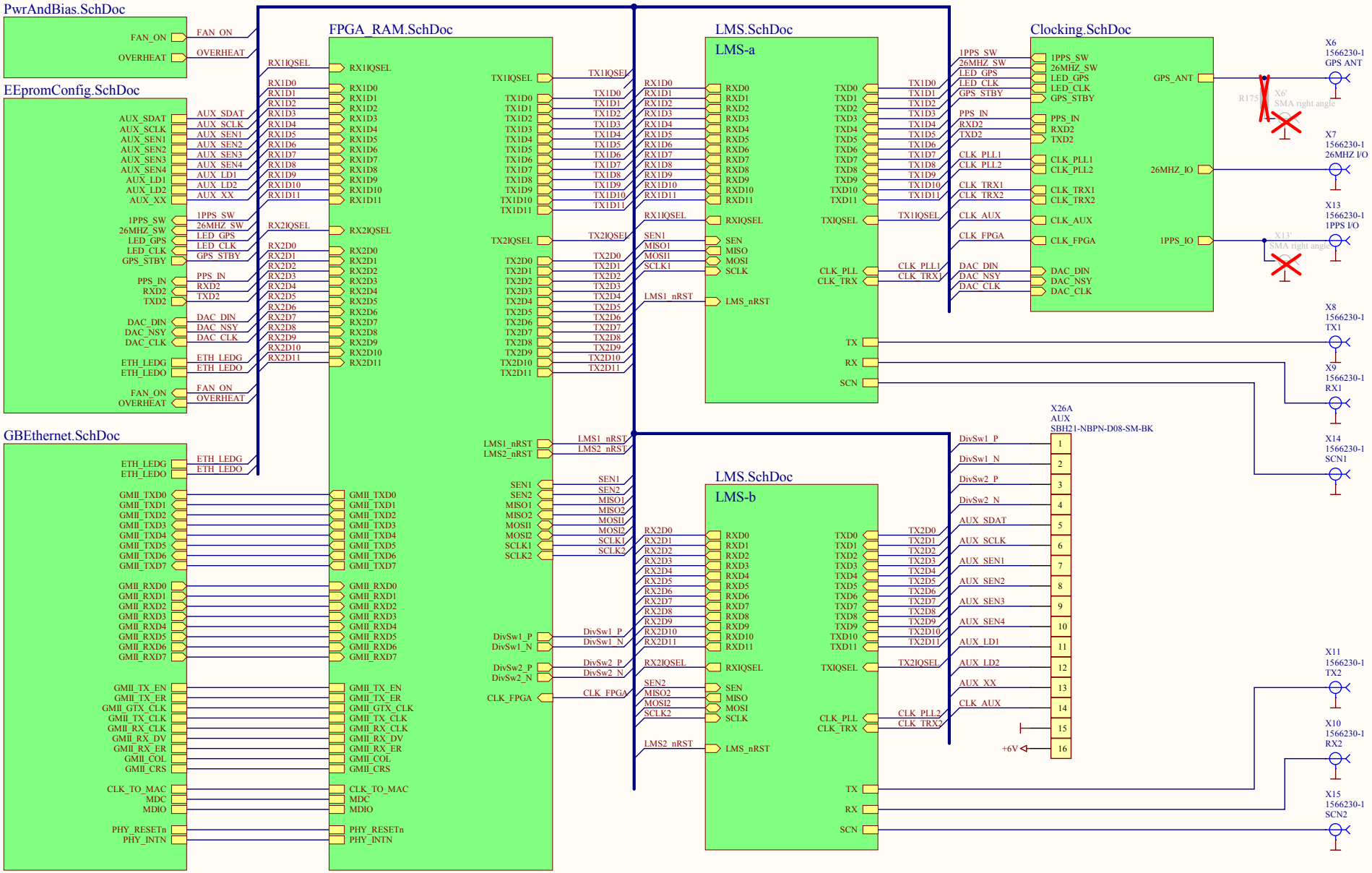
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FAN_ON
OVERHEAT
EEpromConfig.SchDoc
AUX_SDAT
AUX_SCLK
AUX_SEN1
AUX_SEN2
AUX_SEN3
AUX_SEN4
AUX_LD1
AUX_LD2
AUX_XX
1PPS_SW
26MHZ_SW
LED_GPS
LED_CLK
GPS_STBY
PPS_IN
RXD2
TXD2
DAC_DIN
DAC_NSY
DAC_CLK
ETH_LEDG
ETH_LEDO
GBEthernet.SchDoc
GMII_TXD0
GMII_TXD1
GMII_TXD2
GMII_TXD3
GMII_TXD4
GMII_TXD5
GMII_TXD6
GMII_TXD7
GMII_RXD0
GMII_RXD1
GMII_RXD2
GMII_RXD3
GMII_RXD4
GMII_RXD5
GMII_RXD6
GMII_RXD7
GMII_TX_EN
GMII_TX_ER
GMII_GTX_CLK
GMII_TX_CLK
GMII_RX_CLK
GMII_RX_DV
GMII_RX_ER
GMII_COL
GMII_CRS
CLK_TO_MAC
MDC
MDIO
PHY_RESETn
PHY_INTN
FPGA_RAM.SchDoc
RX1IQSEL
RX1D0
RX1D1
RX1D2
RX1D3
RX1D4
RX1D5
RX1D6
RX1D7
RX1D8
RX1D9
RX1D10
RX1D11
RX2IQSEL
RX2D0
RX2D1
RX2D2
RX2D3
RX2D4
RX2D5
RX2D6
RX2D7
RX2D8
RX2D9
RX2D10
RX2D11
TX1IQSEL
TX1D0
TX1D1
TX1D2
TX1D3
TX1D4
TX1D5
TX1D6
TX1D7
TX1D8
TX1D9
TX1D10
TX1D11
TX2IQSEL
TX2D0
TX2D1
TX2D2
TX2D3
TX2D4
TX2D5
TX2D6
TX2D7
TX2D8
TX2D9
TX2D10
TX2D11
LMS1_nRST
LMS2_nRST
SEN1
SEN2
MISO1
MISO2
MOSI1
MOSI2
SCLK1
SCLK2
DivSw1_P
DivSw1_N
DivSw2_P
DivSw2_N
CLK_FPGA
LMS.SchDoc
LMS-a
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
RXD8
RXD9
RXD10
RXD11
RXIQSEL
SEN
MISO
MOSI
SCLK
LMS_nRST
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
TXD8
TXD9
TXD10
TXD11
TXIQSEL
CLK_PLL
CLK_TRX
TX
RX
SCN
LMS-b
Clocking.SchDoc
1PPS_SW
26MHZ_SW
LED_GPS
LED_CLK
GPS_STBY
PPS_IN
RXD2
TXD2
CLK_PLL1
CLK_PLL2
CLK_TRX1
CLK_TRX2
CLK_AUX
CLK_FPGA
DAC_DIN
DAC_NSY
DAC_CLK
GPS_ANT
26MHZ_IO
1PPS_IO
X6
1566230-1
GPS ANT
R175
X6'
SMA right angle
X7
1566230-1
26MHZ I/O
X13
1566230-1
1PPS I/O
X13'
SMA right angle
X8
1566230-1
TX1
X9
1566230-1
RX1
X14
1566230-1
SCN1
X26A
AUX
SBH21-NBPN-D08-SM-BK
DivSw1_P
DivSw1_N
DivSw2_P
DivSw2_N
AUX_SDAT
AUX_SCLK
AUX_SEN1
AUX_SEN2
AUX_SEN3
AUX_SEN4
AUX_LD1
AUX_LD2
AUX_XX
AUX_CLK
+6V
X11
1566230-1
TX2
X10
1566230-1
RX2
X15
1566230-1
SCN2
Title
UmTRXv2_20dBm_TCXO
Size
A3
Number
Revision
1
Date:
10.06.2012
Sheet 1 of 8
File:
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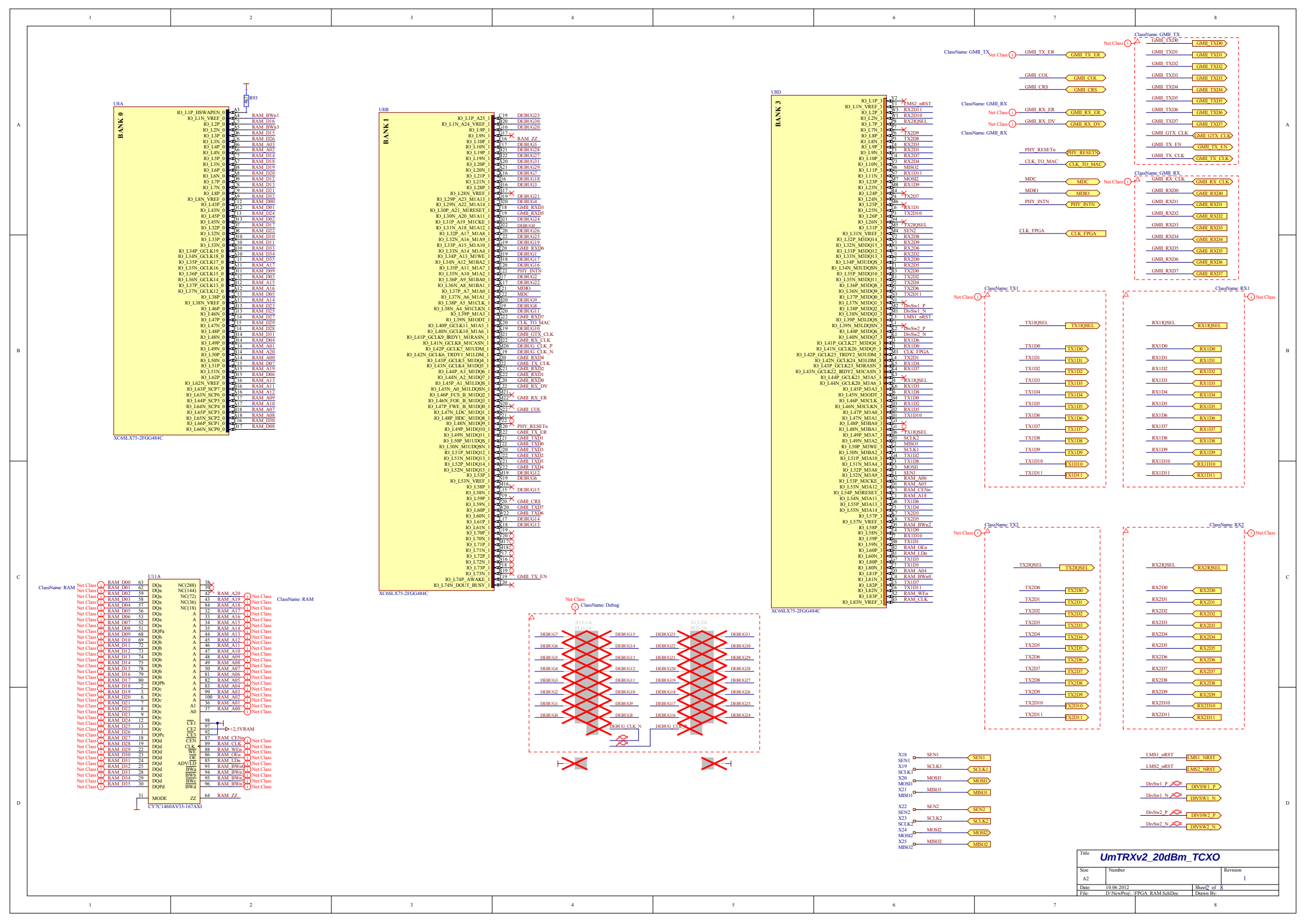
U8A
BANK 0
XC6SLX75-2FGG484C
R93
RAM_BWn1
RAM_D16
RAM_BWn3
RAM_D15
RAM_D26
RAM_A03
RAM_A02
RAM_D14
RAM_D18
RAM_D19
RAM_D20
RAM_D12
RAM_D13
RAM_D21
RAM_D32
RAM_D00
RAM_D01
RAM_D24
RAM_D02
RAM_D17
RAM_D22
RAM_D10
RAM_D11
RAM_D33
RAM_D34
RAM_D35
RAM_A17
RAM_D09
RAM_D03
RAM_A15
RAM_A16
RAM_D23
RAM_D25
RAM_D27
RAM_D29
RAM_D28
RAM_D31
RAM_D04
RAM_A01
RAM_A20
RAM_A00
RAM_D07
RAM_A19
RAM_D06
RAM_A13
RAM_A11
RAM_A12
RAM_A09
RAM_A10
RAM_A07
RAM_A08
RAM_D30
RAM_D08
U8B
BANK 1
XC6SLX75-2FGG484C
DEBUG23
DEBUG30
DEBUG20
RAM_ZZ
DEBUG5
DEBUG28
DEBUG27
DEBUG31
DEBUG29
DEBUG7
DEBUG18
DEBUG3
DEBUG21
DEBUG4
GMII_RXD3
GMII_RXD5
DEBUG24
DEBUG0
DEBUG26
DEBUG25
GMII_RXD6
DEBUG1
DEBUG17
DEBUG16
PHY_INTN
DEBUG2
DEBUG22
MDIO
MDC
DEBUG9
DEBUG8
DEBUG11
GMII_RXD7
CLK_TO_MAC
DEBUG10
GMII_GTX_CLK
GMII_RX_CLK
DEBUG_CLK_P
DEBUG_CLK_N
GMII_RXD4
GMII_TX_CLK
GMII_RXD2
GMII_RXD1
GMII_RXD0
GMII_RX_DV
GMII_RX_ER
GMII_COL
PHY_RESETn
GMII_TX_ER
GMII_TXD0
GMII_TXD3
GMII_TXD5
GMII_TXD4
DEBUG12
DEBUG6
GMII_TXD6
DEBUG14
DEBUG13
DEBUG15
GMII_CRS
GMII_TXD7
DEBUG19
GMII_TX_EN
U8D
BANK 3
XC6SLX75-2FGG484C
X2
RMS2_nRST
RX2D11
RX2D10
RX2IQSEL
TX2D9
TX2D8
RX2D3
RX2D1
RX2D7
RX2D4
MISO2
RX1D11
MOSI2
RX1D9
TX2D7
RX1D1
TX2D10
TX2D6
TX2IQSEL
SEN2
RX2D8
RX2D9
RX2D6
RX2D2
RX2D0
RX2D5
TX2D0
TX2D2
TX2D4
TX2D5
TX2D1
TX2D3
DivSw1_P
DivSw1_N
LMS1_nRST
DivSw2_P
DivSw2_N
RX1D6
CLK_FPGA
RX1D4
RX1D7
RX1IQSEL
RX1D3
RX1D8
RX1D2
RX1D5
TX1D10
TX2IQSEL
SCLK2
MISO1
SCLK1
TX1D2
TX1D8
MOSI1
SEN1
RAM_A06
RAM_A05
RAM_CENn
RAM_A18
TX1D6
TX1D4
TX2D3
TX2D5
RAM_BWn2
TX1D9
RX1D10
TX1D1
RAM_OEn
RAM_LDn
TX1D3
TX1D5
RAM_A04
RAM_BWn0
TX1D7
TX1D11
RAM_WEn
RAM_CLK
ClassName: GMII_TX
GMII_TX_ER
GMII_COL
GMII_CRS
ClassName: GMII_RX
GMII_RX_ER
GMII_RX_DV
PHY_RESETn
CLK_TO_MAC
MDC
MDIO
PHY_INTN
CLK_FPGA
GMII_TXD0
GMII_TXD1
GMII_TXD2
GMII_TXD3
GMII_TXD4
GMII_TXD5
GMII_TXD6
GMII_TXD7
GMII_GTX_CLK
GMII_TX_EN
GMII_TX_CLK
GMII_RX_CLK
GMII_RXD0
GMII_RXD1
GMII_RXD2
GMII_RXD3
GMII_RXD4
GMII_RXD5
GMII_RXD6
GMII_RXD7
ClassName: TX1
TX1IQSEL
TX1D0
TX1D1
TX1D2
TX1D3
TX1D4
TX1D5
TX1D6
TX1D7
TX1D8
TX1D9
TX1D10
TX1D11
ClassName: RX1
RX1IQSEL
RX1D0
RX1D1
RX1D2
RX1D3
RX1D4
RX1D5
RX1D6
RX1D7
RX1D8
RX1D9
RX1D10
RX1D11
ClassName: TX2
TX2IQSEL
TX2D0
TX2D1
TX2D2
TX2D3
TX2D4
TX2D5
TX2D6
TX2D7
TX2D8
TX2D9
TX2D10
TX2D11
ClassName: RX2
RX2IQSEL
RX2D0
RX2D1
RX2D2
RX2D3
RX2D4
RX2D5
RX2D6
RX2D7
RX2D8
RX2D9
RX2D10
RX2D11
ClassName: RAM
U11A
CY7C1460AV33-167AXI
RAM_D00
RAM_D01
RAM_D02
RAM_D03
RAM_D04
RAM_D05
RAM_D06
RAM_D07
RAM_D08
RAM_D09
RAM_D10
RAM_D11
RAM_D12
RAM_D13
RAM_D14
RAM_D15
RAM_D16
RAM_D17
RAM_D18
RAM_D19
RAM_D20
RAM_D21
RAM_D22
RAM_D23
RAM_D24
RAM_D25
RAM_D26
RAM_D27
RAM_D28
RAM_D29
RAM_D30
RAM_D31
RAM_D32
RAM_D33
RAM_D34
RAM_D35
MODE
ZZ
RAM_A20
RAM_A19
RAM_A18
RAM_A17
RAM_A16
RAM_A15
RAM_A14
RAM_A13
RAM_A12
RAM_A11
RAM_A10
RAM_A09
RAM_A08
RAM_A07
RAM_A06
RAM_A05
RAM_A04
RAM_A03
RAM_A02
RAM_A01
RAM_A00
+2_5VRAM
RAM_CENn
RAM_CLK
RAM_WEn
RAM_OEn
RAM_LDn
RAM_BWn0
RAM_BWn1
RAM_BWn2
RAM_BWn3
RAM_ZZ
ClassName: Debug
X13-1A
X13-2A
DEBUG7
DEBUG6
DEBUG5
DEBUG4
DEBUG3
DEBUG2
DEBUG1
DEBUG0
DEBUG15
DEBUG14
DEBUG13
DEBUG12
DEBUG11
DEBUG10
DEBUG9
DEBUG8
DEBUG_CLK_N
DEBUG_CLK_P
DEBUG23
DEBUG22
DEBUG21
DEBUG20
DEBUG19
DEBUG18
DEBUG17
DEBUG16
DEBUG31
DEBUG30
DEBUG29
DEBUG28
DEBUG27
DEBUG26
DEBUG25
DEBUG24
X18
SEN1
X19
SCLK1
X20
MOSI1
X21
MISO1
X22
SEN2
X23
SCLK2
X24
MOSI2
X25
MISO2
LMS1_nRST
LMS2_nRST
DivSw1_P
DivSw1_N
DivSw2_P
DivSw2_N
Title
UmTRXv2_20dBm_TCXO
Size
A2
Number
Revision
1
Date:
10.06.2012
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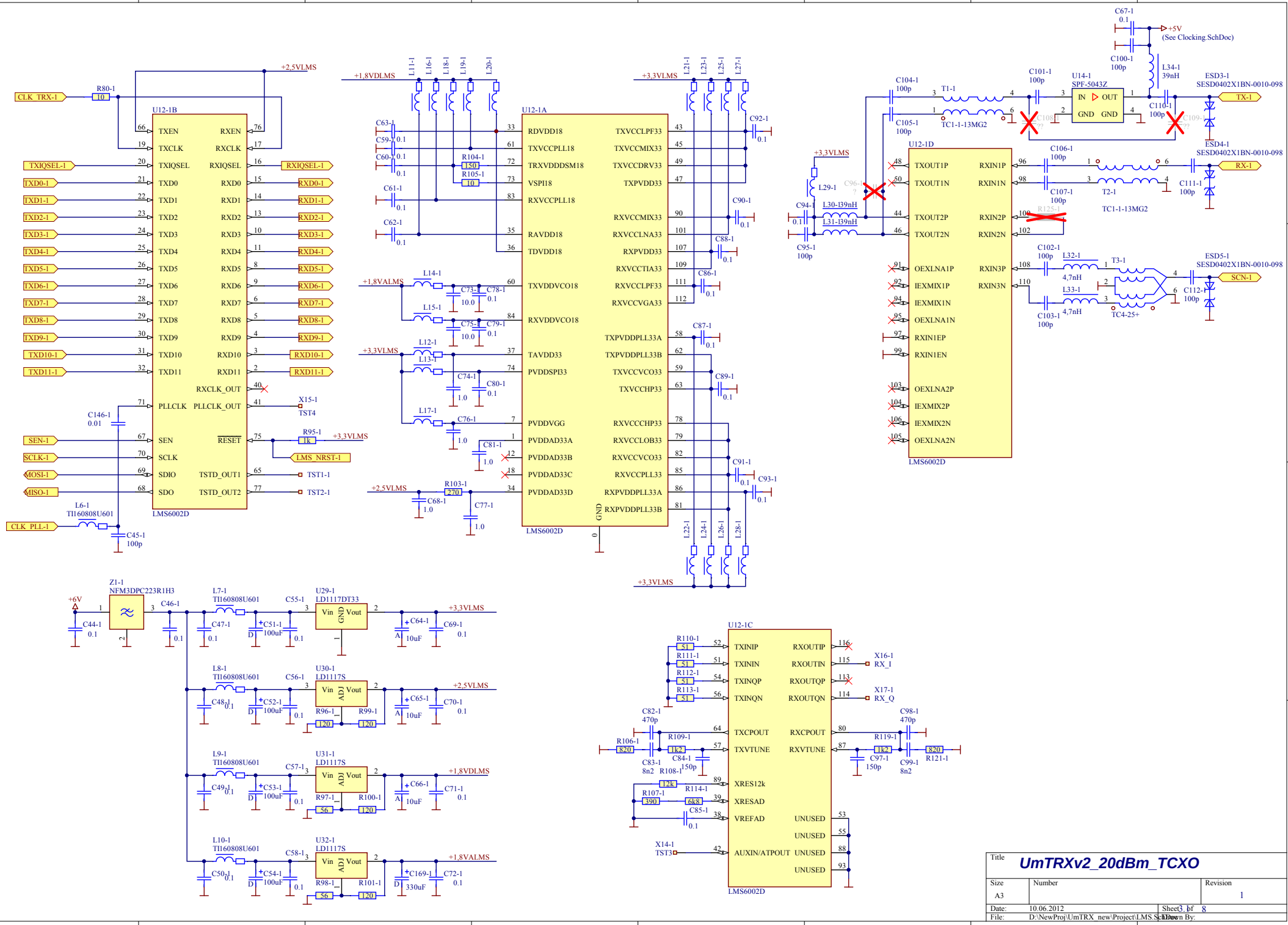

U12-1B
LMS6002D
U12-1A
LMS6002D
U12-1D
LMS6002D
U12-1C
LMS6002D
U14-1
SPF-5043Z
IN
OUT
GND
GND
+5V
(See Clocking.SchDoc)
ESD3-1
SESD0402X1BN-0010-098
ESD4-1
SESD0402X1BN-0010-098
ESD5-1
SESD0402X1BN-0010-098
TX-1
RX-1
SCN-1
TC1-1-13MG2
TC4-25+
CLK_TRX-1
CLK_PLL-1
TXIQSEL-1
RXIQSEL-1
SEN-1
SCLK-1
MOSI-1
MISO-1
LMS_NRST-1
TST1-1
TST2-1
TST4
+2,5VLMS
+1,8VDLMS
+1,8VALMS
+3,3VLMS
+6V
Z1-1
NFM3DPC223R1H3
U29-1
LD1117DT33
U30-1
LD1117S
U31-1
LD1117S
U32-1
LD1117S
TI160808U601
X16-1
RX_I
X17-1
RX_Q
X14-1
TST3
Title
UmTRXv2_20dBm_TCXO
Size
A3
Number
Revision
1
Date:
10.06.2012
Sheet 3 of 8
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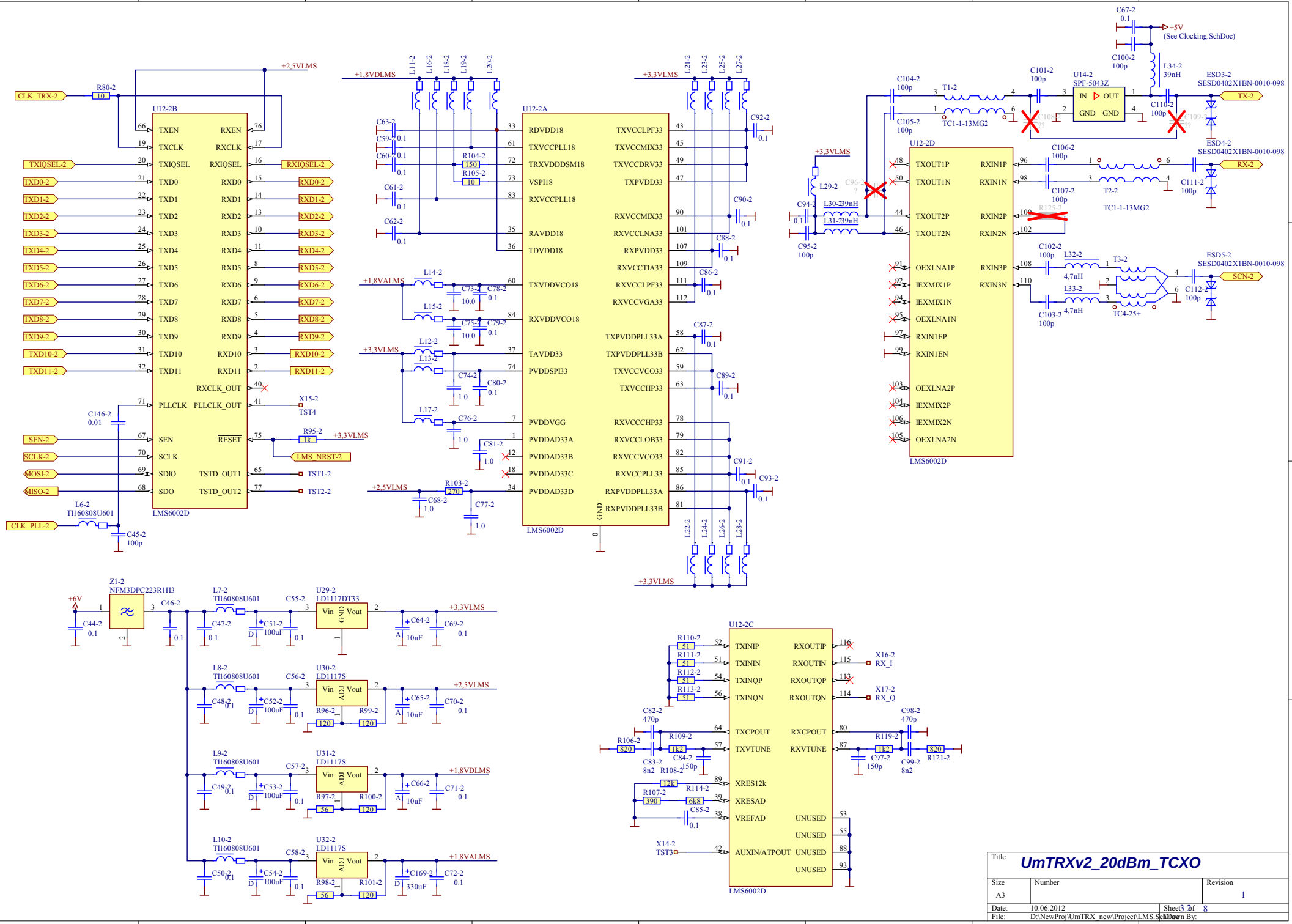
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U12-2A
LMS6002D
U12-2D
LMS6002D
U12-2C
LMS6002D
CLK_TRX-2
TXIQSEL-2
TXD0-2
TXD1-2
TXD2-2
TXD3-2
TXD4-2
TXD5-2
TXD6-2
TXD7-2
TXD8-2
TXD9-2
TXD10-2
TXD11-2
SEN-2
SCLK-2
MOSI-2
MISO-2
CLK_PLL-2
RXIQSEL-2
RXD0-2
RXD1-2
RXD2-2
RXD3-2
RXD4-2
RXD5-2
RXD6-2
RXD7-2
RXD8-2
RXD9-2
RXD10-2
RXD11-2
LMS_NRST-2
TST1-2
TST2-2
TX-2
RX-2
SCN-2
+2,5VLMS
+1,8VDLMS
+1,8VALMS
+3,3VLMS
+6V
+5V
(See Clocking.SchDoc)
Title
UmTRXv2_20dBm_TCXO
Size
A3
Number
Revision
1
Date:
10.06.2012
Sheet 3 of 8
File:
D:\NewProj\UmTRX_new\Project\LMS.SchDoc
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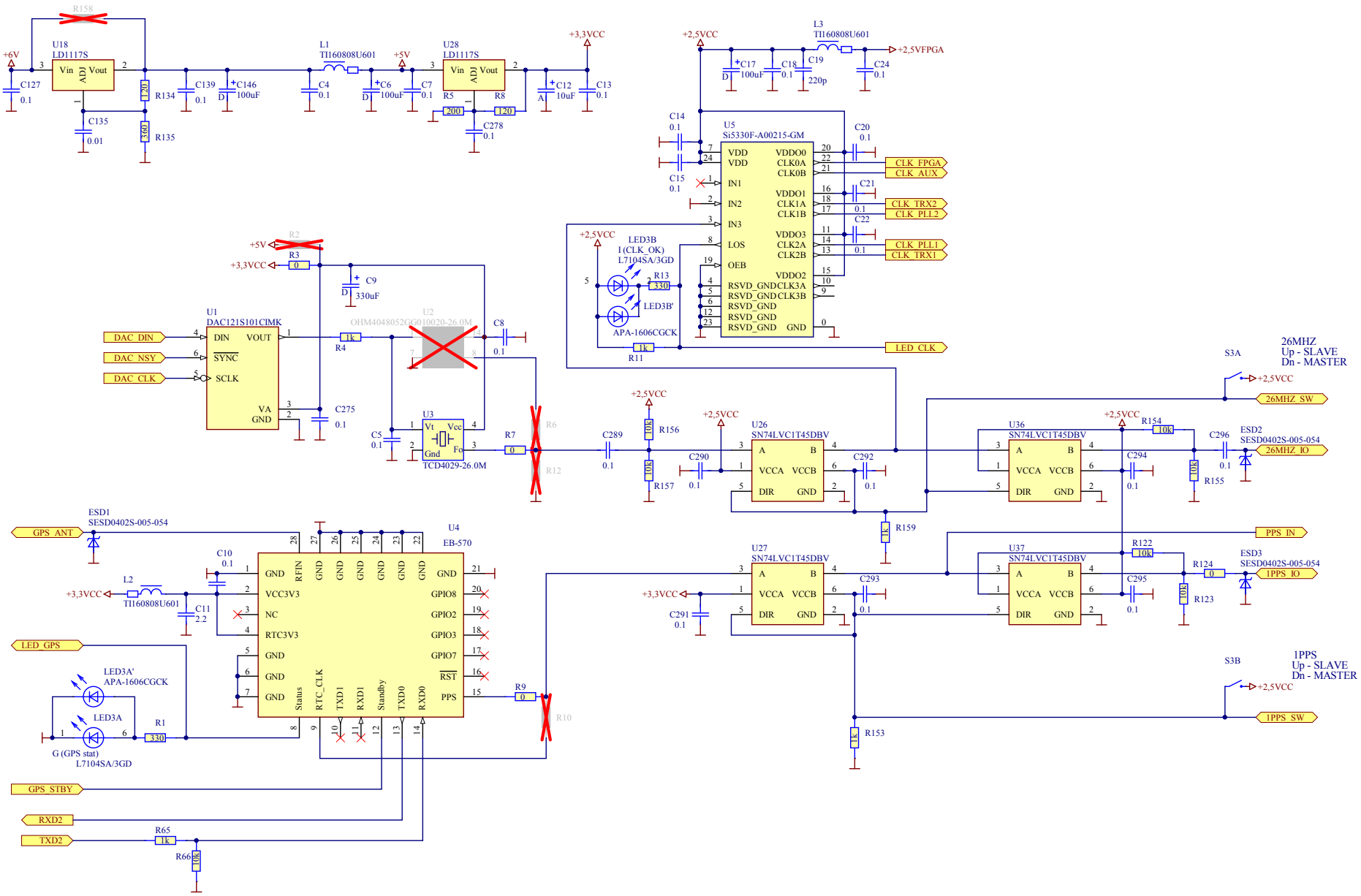

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Date: 10.06.2012	Sheet 5 of 8	
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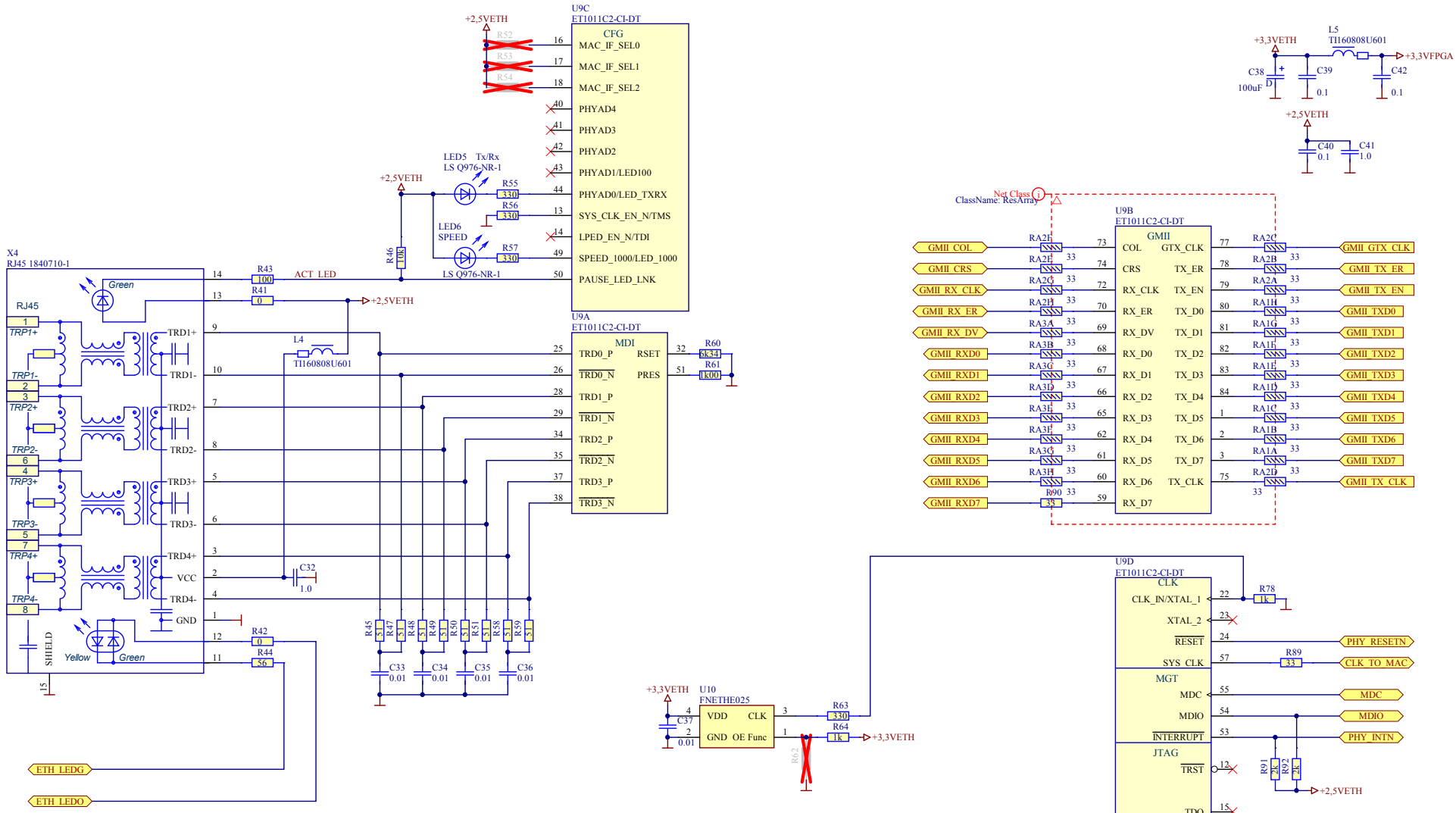

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Date: 10.06.2012		Sheet 6 of 8
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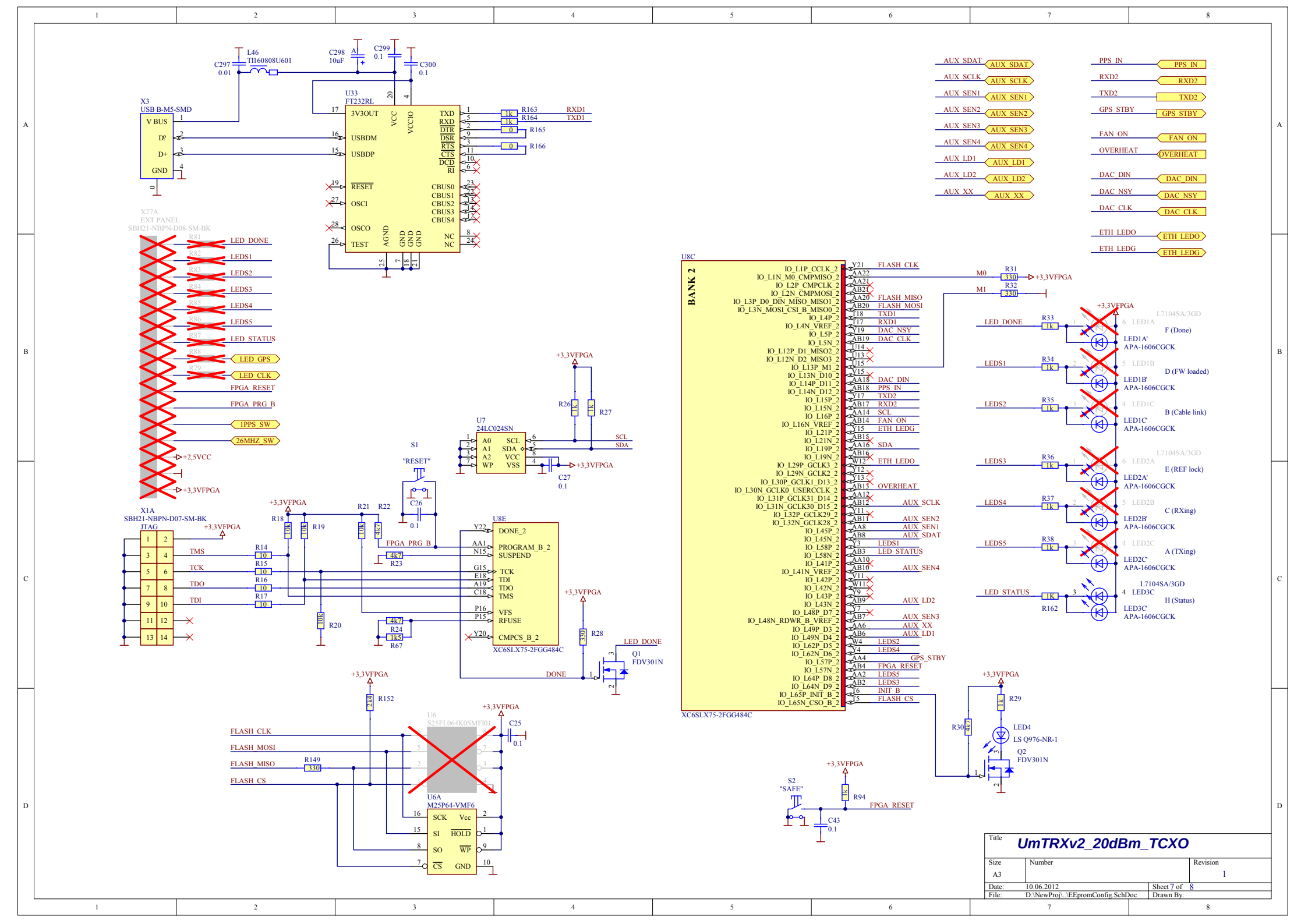
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TI160808U601
C297
0.01
C298
10uF
C299
0.1
C300
0.1
X3
USB B-M5-SMD
V BUS
D?
D+
GND
U33
FT232RL
3V3OUT
USBDM
USBDP
RESET
OSCI
OSCO
TEST
VCC
VCCIO
AGND
GND
TXD
RXD
DTR
DSR
RTS
CTS
DCD
RI
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
NC
R163
R164
R165
R166
RXD1
TXD1
X27A
EXT PANEL
SBH21-NBPN-D08-SM-BK
LED_DONE
LEDS1
LEDS2
LEDS3
LEDS4
LEDS5
LED_STATUS
LED_GPS
LED_CLK
FPGA_RESET
FPGA_PRG_B
1PPS_SW
26MHZ_SW
+2,5VCC
+3,3VFPGA
U7
24LC024SN
A0
A1
A2
WP
SCL
SDA
VCC
VSS
R26
R27
C27
0.1
S1
"RESET"
C26
0.1
X1A
SBH21-NBPN-D07-SM-BK
JTAG
TMS
TCK
TDO
TDI
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R67
FPGA_PRG_B
U8E
DONE_2
PROGRAM_B_2
SUSPEND
TCK
TDI
TDO
TMS
VFS
RFUSE
CMPCS_B_2
XC6SLX75-2FGG484C
R28
Q1
FDV301N
LED_DONE
DONE
R152
U6
S25FL064K0SMFI01
U6A
M25P64-VMF6
FLASH_CLK
FLASH_MOSI
FLASH_MISO
FLASH_CS
R149
C25
0.1
SCK
SI
SO
CS
Vcc
HOLD
WP
GND
U8C
BANK 2
IO_L1P_CCLK_2
IO_L1N_M0_CMPMISO_2
IO_L2P_CMPCLK_2
IO_L2N_CMPMOSI_2
IO_L3P_D0_DIN_MISO_MISO1_2
IO_L3N_MOSI_CSI_B_MISO0_2
IO_L4P_2
IO_L4N_VREF_2
IO_L5P_2
IO_L5N_2
IO_L12P_D1_MISO2_2
IO_L12N_D2_MISO3_2
IO_L13P_M1_2
IO_L13N_D10_2
IO_L14P_D11_2
IO_L14N_D12_2
IO_L15P_2
IO_L15N_2
IO_L16P_2
IO_L16N_VREF_2
IO_L21P_2
IO_L21N_2
IO_L19P_2
IO_L19N_2
IO_L29P_GCLK3_2
IO_L29N_GCLK2_2
IO_L30P_GCLK1_D13_2
IO_L30N_GCLK0_USERCCLK_2
IO_L31P_GCLK31_D14_2
IO_L31N_GCLK30_D15_2
IO_L32P_GCLK29_2
IO_L32N_GCLK28_2
IO_L45P_2
IO_L45N_2
IO_L58P_2
IO_L58N_2
IO_L41P_2
IO_L41N_VREF_2
IO_L42P_2
IO_L42N_2
IO_L43P_2
IO_L43N_2
IO_L48P_D7_2
IO_L48N_RDWR_B_VREF_2
IO_L49P_D3_2
IO_L49N_D4_2
IO_L62P_D5_2
IO_L62N_D6_2
IO_L57P_2
IO_L57N_2
IO_L64P_D8_2
IO_L64N_D9_2
IO_L65P_INIT_B_2
IO_L65N_CSO_B_2
FLASH_CLK
FLASH_MISO
FLASH_MOSI
TXD1
RXD1
DAC_NSY
DAC_CLK
DAC_DIN
PPS_IN
TXD2
SCL
FAN_ON
ETH_LEDG
SDA
ETH_LEDO
OVERHEAT
AUX_SCLK
AUX_SEN2
AUX_SEN1
AUX_SDAT
LED1
AUX_SEN4
AUX_LD2
AUX_SEN3
AUX_XX
GPS_STBY
FPGA_RESET
LEDS5
LEDS3
INIT_B
FLASH_CS
XC6SLX75-2FGG484C
M0
M1
R31
R32
+3,3VFPGA
LED_DONE
LEDS1
LEDS2
LEDS3
LEDS4
LEDS5
LED_STATUS
R33
R34
R35
R36
R37
R38
R162
L7104SA/3GD
LED1A
LED1A'
APA-1606CGCK
F (Done)
LED1B
LED1B'
D (FW loaded)
LED1C
LED1C'
B (Cable link)
LED2A
LED2A'
E (REF lock)
LED2B
LED2B'
C (RXing)
LED2C
LED2C'
A (TXing)
LED3C
LED3C'
H (Status)
R29
R30
LED4
LS Q976-NR-1
Q2
FDV301N
S2
"SAFE"
R94
C43
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Title
UmTRXv2_20dBm_TCXO
Size
A3
Number
Revision
1
Date:
10.06.2012
Sheet 7 of 8
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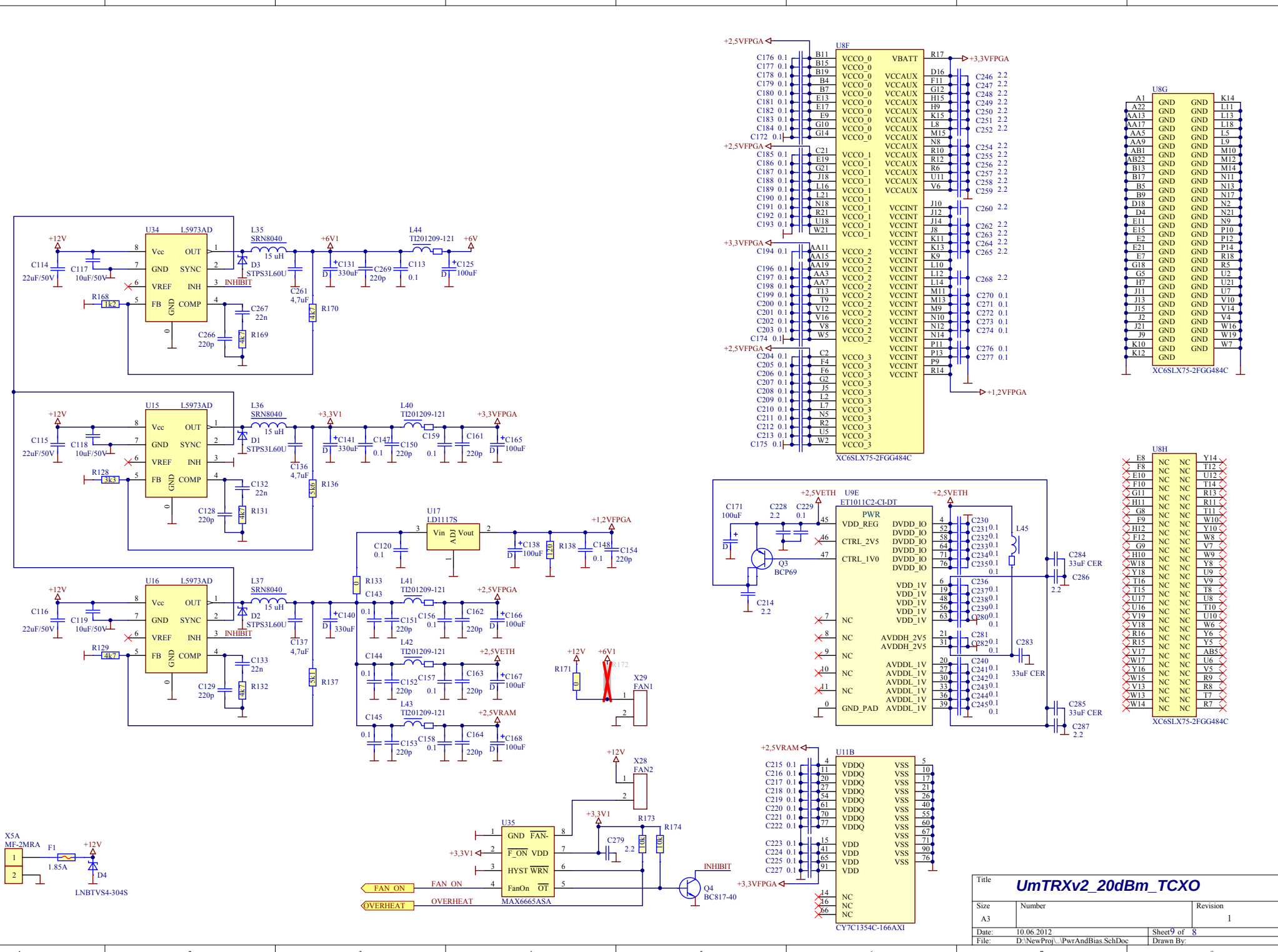
D:\NewProj\..\EEpromConfig.SchDoc
Drawn By:


U34 L5973AD
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U17 LD1117S
U8F
U8G
U8H
U9E ET1011C2-CI-DT
U11B
U35 MAX6665ASA
XC6SLX75-2FGG484C
CY7C1354C-166AXI
Title
UmTRXv2_20dBm_TCXO
Size
A3
Number
Revision
1
Date: 10.06.2012
File: D:\NewProj\..\PwrAndBias.SchDoc
Sheet 9 of 8
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