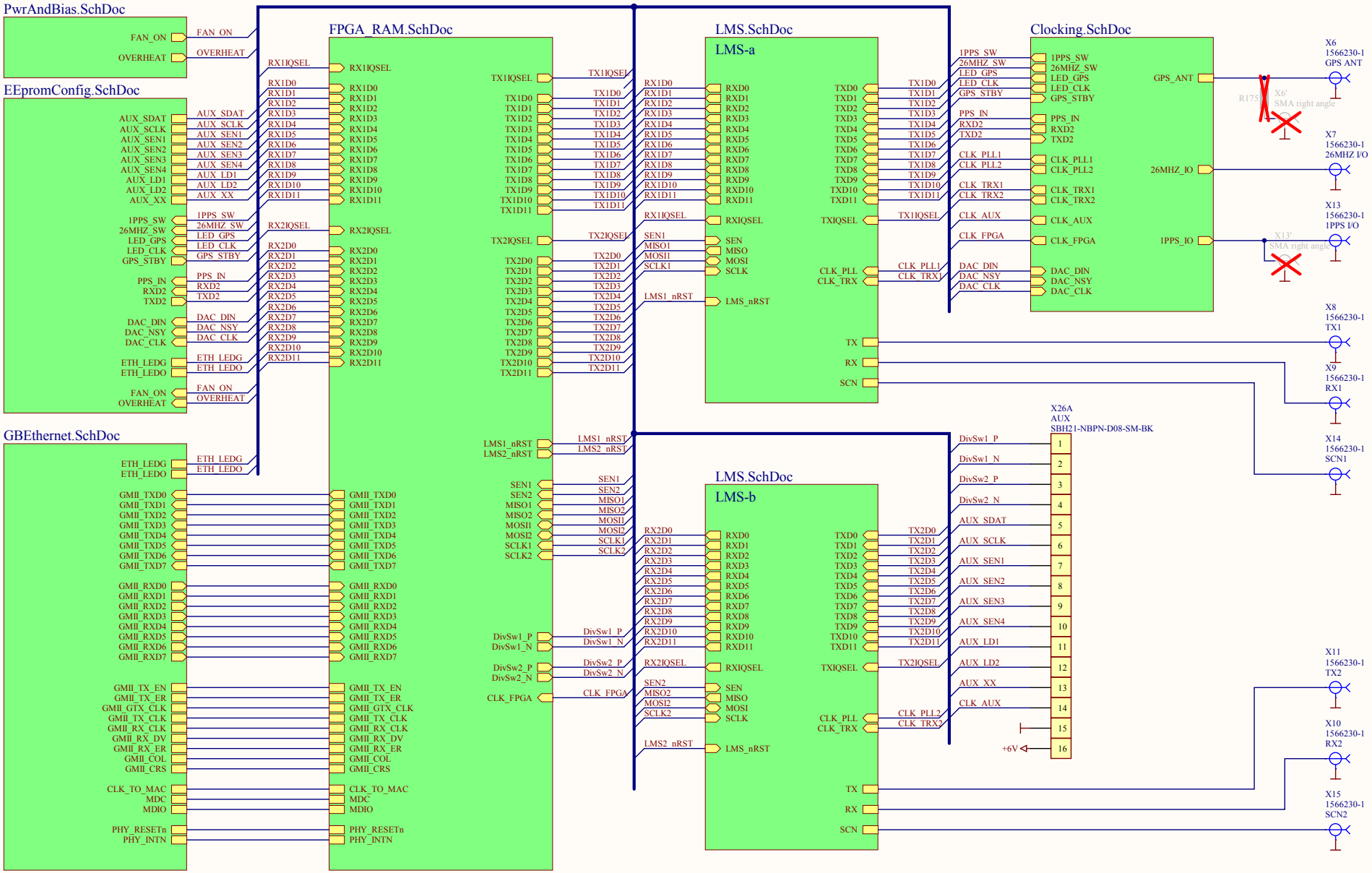

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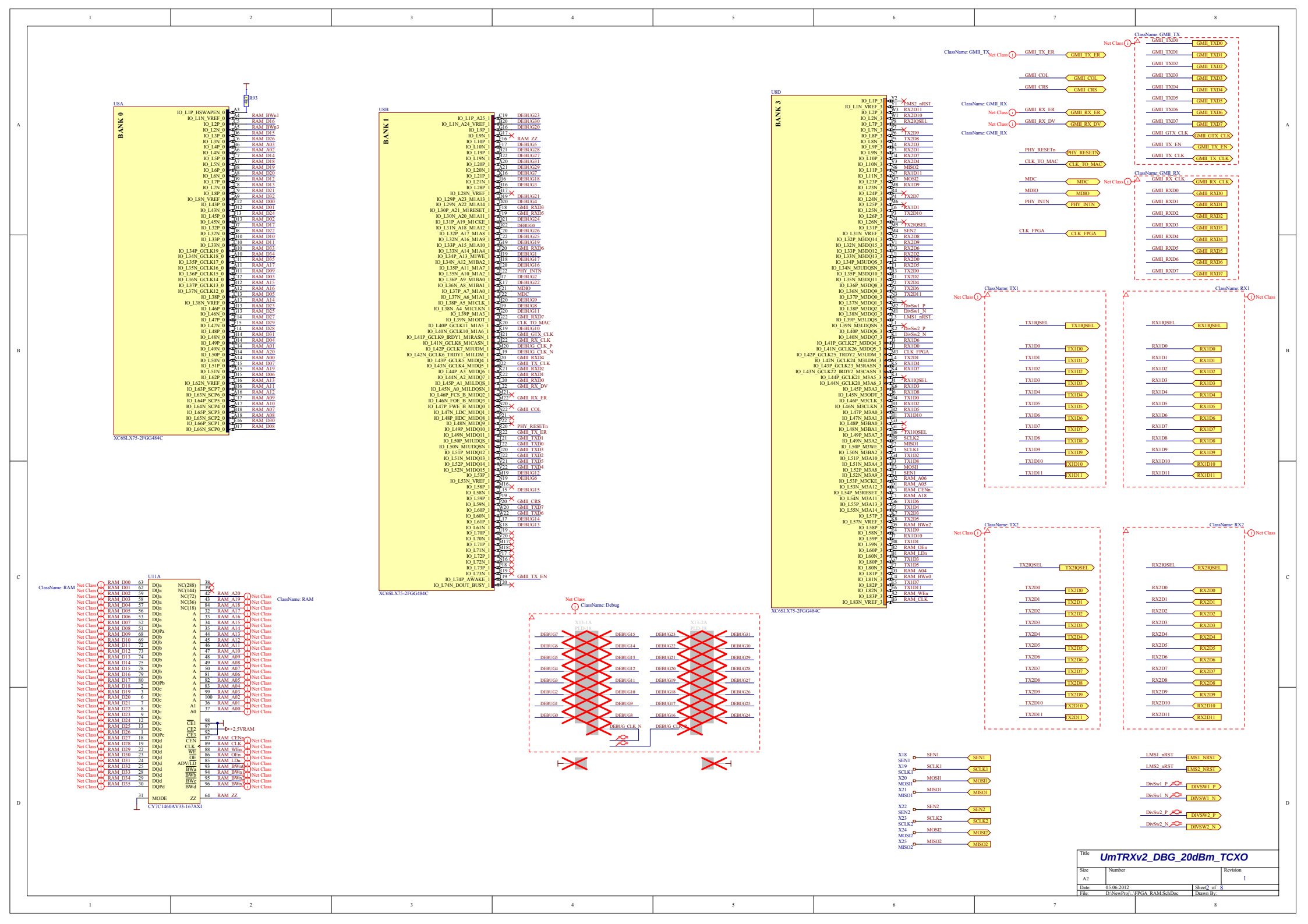
Date: 05.06.2012	Sheet 1 of 8	
File: D:\NewProj\..\Total.SchDoc	Drawn By:	


U8A
BANK 0
XC6SLX75-2FGG484C
R93
RAM_BWn1
RAM_D16
RAM_BWn3
RAM_D15
RAM_D26
RAM_A03
RAM_A02
RAM_D14
RAM_D18
RAM_D19
RAM_D20
RAM_D12
RAM_D13
RAM_D21
RAM_D32
RAM_D00
RAM_D01
RAM_D24
RAM_D02
RAM_D17
RAM_D22
RAM_D10
RAM_D11
RAM_D33
RAM_D34
RAM_D35
RAM_A17
RAM_D09
RAM_D03
RAM_A15
RAM_A16
RAM_D05
RAM_D25
RAM_D27
RAM_D29
RAM_D28
RAM_D31
RAM_D04
RAM_A01
RAM_A20
RAM_A00
RAM_D07
RAM_A19
RAM_D06
RAM_A13
RAM_A11
RAM_A12
RAM_A09
RAM_A10
RAM_A07
RAM_A08
RAM_D30
RAM_D08
U8B
BANK 1
XC6SLX75-2FGG484C
DEBUG23
DEBUG30
DEBUG20
RAM_ZZ
DEBUG5
DEBUG28
DEBUG27
DEBUG31
DEBUG29
DEBUG7
DEBUG18
DEBUG3
DEBUG21
DEBUG4
GMII_RXD3
GMII_RXD5
DEBUG24
DEBUG0
DEBUG26
DEBUG25
GMII_RXD6
DEBUG1
DEBUG17
DEBUG16
PHY_INTN
DEBUG2
DEBUG22
MDIO
MDC
DEBUG9
DEBUG8
DEBUG11
GMII_RXD7
CLK_TO_MAC
DEBUG10
GMII_GTX_CLK
GMII_RX_CLK
DEBUG_CLK_P
DEBUG_CLK_N
GMII_RXD4
GMII_TX_CLK
GMII_RXD2
GMII_RXD1
GMII_RXD0
GMII_RX_DV
GMII_RX_ER
GMII_COL
PHY_RESETn
GMII_TX_ER
GMII_TXD0
GMII_TXD3
GMII_TXD5
GMII_TXD4
DEBUG12
DEBUG6
GMII_TXD6
DEBUG14
DEBUG13
DEBUG15
GMII_CRS
GMII_TXD7
GMII_TX_EN
U8D
BANK 3
XC6SLX75-2FGG484C
X2
TMS2_nRST
RX2D11
RX2D10
RX2IQSEL
TX2D9
TX2D8
RX2D3
RX2D1
RX2D7
RX2D4
MISO2
RX1D11
TX2D7
RX1D9
TX2D3
RX1D1
TX2D10
TX2IQSEL
SEN2
RX2D8
RX2D9
RX2D6
RX2D2
RX2D0
TX2D0
TX2D2
TX2D1
TX2D4
TX2D6
TX2D5
TX2D11
DivSw1_P
DivSw1_N
LMS1_nRST
DivSw2_P
DivSw2_N
RX1D6
CLK_FPGA
RX1D4
RX1D7
RX1D3
RX1D8
TX1D0
RX1D5
TX1D10
TX1IQSEL
SCLK2
MISO1
SCLK1
TX1D2
TX1D8
MOSI1
SEN1
RAM_A06
RAM_A05
RAM_CENn
RAM_A18
TX1D6
TX1D4
TX2D3
TX2D5
RAM_BWn2
TX1D9
RX1D10
TX1D1
RAM_OEn
RAM_LDn
TX1D3
TX1D5
RAM_A04
RAM_BWn0
TX1D7
TX1D11
RAM_WEn
RAM_CLK
ClassName: GMII_TX
GMII_TX_ER
GMII_COL
GMII_CRS
ClassName: GMII_RX
GMII_RX_ER
GMII_RX_DV
PHY_RESETn
CLK_TO_MAC
MDC
MDIO
PHY_INTN
CLK_FPGA
GMII_TXD0
GMII_TXD1
GMII_TXD2
GMII_TXD3
GMII_TXD4
GMII_TXD5
GMII_TXD6
GMII_TXD7
GMII_GTX_CLK
GMII_TX_EN
GMII_TX_CLK
GMII_RX_CLK
GMII_RXD0
GMII_RXD1
GMII_RXD2
GMII_RXD3
GMII_RXD4
GMII_RXD5
GMII_RXD6
GMII_RXD7
ClassName: TX1
ClassName: RX1
ClassName: TX2
ClassName: RX2
TX1IQSEL
TX1D0
TX1D1
TX1D2
TX1D3
TX1D4
TX1D5
TX1D6
TX1D7
TX1D8
TX1D9
TX1D10
TX1D11
RX1IQSEL
RX1D0
RX1D1
RX1D2
RX1D3
RX1D4
RX1D5
RX1D6
RX1D7
RX1D8
RX1D9
RX1D10
RX1D11
TX2IQSEL
TX2D0
TX2D1
TX2D2
TX2D3
TX2D4
TX2D5
TX2D6
TX2D7
TX2D8
TX2D9
TX2D10
TX2D11
RX2IQSEL
RX2D0
RX2D1
RX2D2
RX2D3
RX2D4
RX2D5
RX2D6
RX2D7
RX2D8
RX2D9
RX2D10
RX2D11
ClassName: RAM
U11A
CY7C1460AV33-167AXI
RAM_D00
RAM_D01
RAM_D02
RAM_D03
RAM_D04
RAM_D05
RAM_D06
RAM_D07
RAM_D08
RAM_D09
RAM_D10
RAM_D11
RAM_D12
RAM_D13
RAM_D14
RAM_D15
RAM_D16
RAM_D17
RAM_D18
RAM_D19
RAM_D20
RAM_D21
RAM_D22
RAM_D23
RAM_D24
RAM_D25
RAM_D26
RAM_D27
RAM_D28
RAM_D29
RAM_D30
RAM_D31
RAM_D32
RAM_D33
RAM_D34
RAM_D35
MODE
ZZ
+2_5VRAM
RAM_A20
RAM_A19
RAM_A18
RAM_A17
RAM_A16
RAM_A15
RAM_A14
RAM_A13
RAM_A12
RAM_A11
RAM_A10
RAM_A09
RAM_A08
RAM_A07
RAM_A06
RAM_A05
RAM_A04
RAM_A03
RAM_A02
RAM_A01
RAM_A00
RAM_CENn
RAM_CLK
RAM_WEn
RAM_OEn
RAM_LDn
RAM_BWn0
RAM_BWn1
RAM_BWn2
RAM_BWn3
RAM_ZZ
ClassName: Debug
X13-1A
X13-2A
DEBUG7
DEBUG6
DEBUG5
DEBUG4
DEBUG3
DEBUG2
DEBUG1
DEBUG0
DEBUG15
DEBUG14
DEBUG13
DEBUG12
DEBUG11
DEBUG10
DEBUG9
DEBUG8
DEBUG_CLK_N
DEBUG_CLK_P
DEBUG23
DEBUG22
DEBUG21
DEBUG20
DEBUG19
DEBUG18
DEBUG17
DEBUG16
DEBUG31
DEBUG30
DEBUG29
DEBUG28
DEBUG27
DEBUG26
DEBUG25
DEBUG24
X18
SEN1
X19
SCLK1
X20
MOSI1
X21
MISO1
X22
SEN2
X23
SCLK2
X24
MOSI2
X25
MISO2
LMS1_nRST
LMS2_nRST
DivSw1_P
DivSw1_N
DivSw2_P
DivSw2_N
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UmTRXv2_DBG_20dBm_TCXO
Size
A2
Number
Revision
1
Date:
05.06.2012
Sheet2_of_8
File:
D:\NewProj\...\FPGA_RAM.SchDoc
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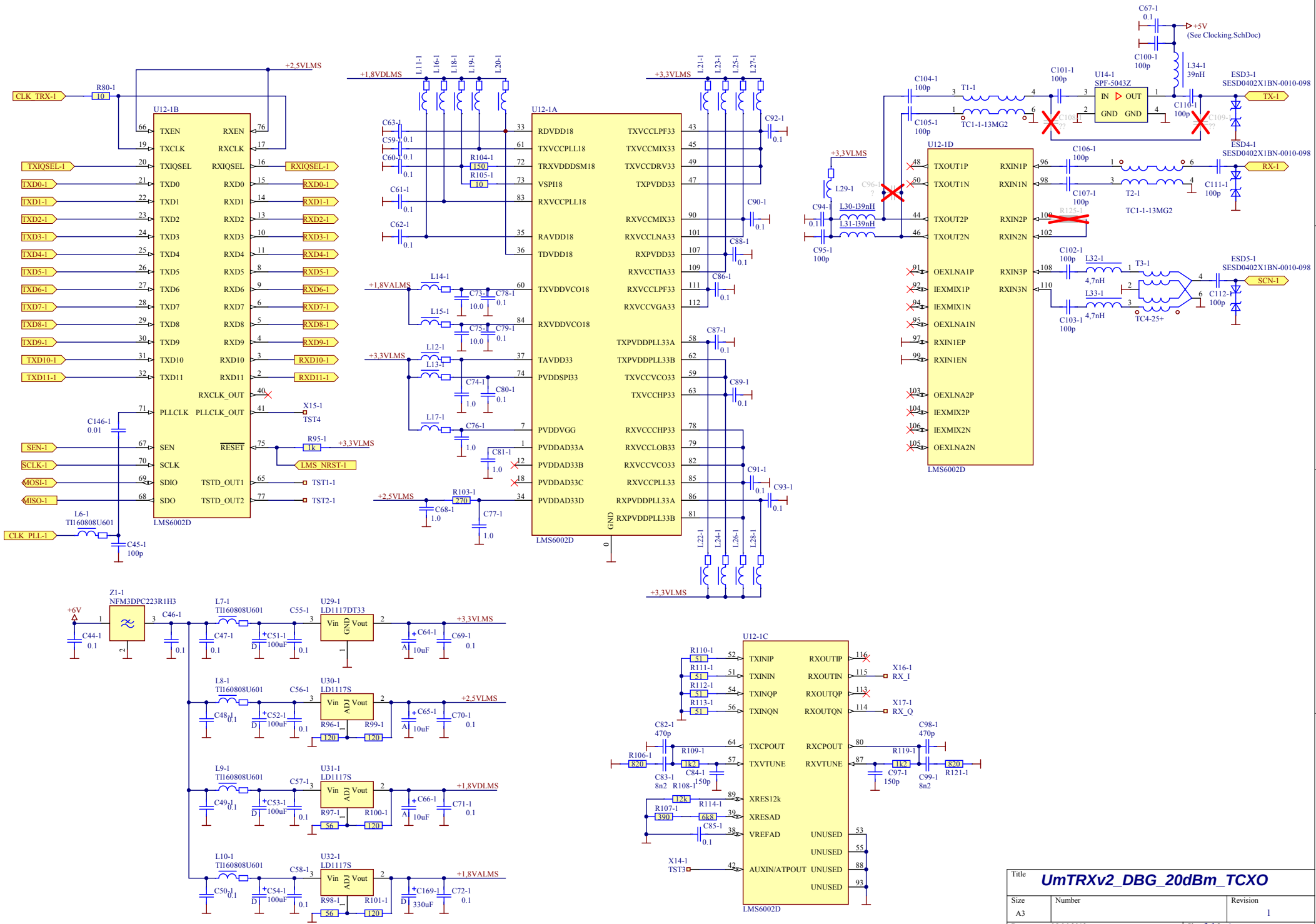
U12-1B
LMS6002D
U12-1A
LMS6002D
U12-1D
LMS6002D
U12-1C
LMS6002D
CLK_TRX-1
R80-1
10
+2,5VLMS
TXIQSEL-1
TXD0-1
TXD1-1
TXD2-1
TXD3-1
TXD4-1
TXD5-1
TXD6-1
TXD7-1
TXD8-1
TXD9-1
TXD10-1
TXD11-1
RXIQSEL-1
RXD0-1
RXD1-1
RXD2-1
RXD3-1
RXD4-1
RXD5-1
RXD6-1
RXD7-1
RXD8-1
RXD9-1
RXD10-1
RXD11-1
C146-1
0.01
SEN-1
SCLK-1
MOSI-1
MISO-1
L6-1
TI160808U601
CLK_PLL-1
C45-1
100p
X15-1
TST4
R95-1
1k
+3,3VLMS
LMS_NRST-1
TST1-1
TST2-1
+1,8VDLMS
+1,8VALMS
+2,5VLMS
+3,3VLMS
C63-1
C59-1
C60-1
C61-1
C62-1
R104-1
150
R105-1
10
L14-1
L15-1
L12-1
L13-1
L17-1
C73-1
C78-1
C75-1
C79-1
C74-1
C80-1
C76-1
C81-1
R103-1
270
C68-1
C77-1
C92-1
C90-1
C88-1
C86-1
C87-1
C89-1
C91-1
C93-1
C67-1
+5V
(See Clocking.SchDoc)
C100-1
100p
L34-1
39nH
C101-1
100p
U14-1
SPF-5043Z
ESD3-1
SESD0402X1BN-0010-098
TX-1
C104-1
100p
T1-1
C105-1
100p
TC1-1-13MG2
C110-1
100p
ESD4-1
SESD0402X1BN-0010-098
RX-1
C106-1
100p
C107-1
100p
T2-1
TC1-1-13MG2
C111-1
100p
C102-1
100p
L32-1
4,7nH
T3-1
ESD5-1
SESD0402X1BN-0010-098
SCN-1
L33-1
4,7nH
C103-1
100p
TC4-25+
C112-1
100p
L29-1
L30-139nH
L31-139nH
C94-1
0.1
C95-1
100p
Z1-1
NFM3DPC223R1H3
+6V
C44-1
0.1
C46-1
0.1
L7-1
TI160808U601
C47-1
0.1
C51-1
100uF
C55-1
0.1
U29-1
LD1117DT33
Vin
GND
Vout
C64-1
10uF
C69-1
0.1
+3,3VLMS
L8-1
TI160808U601
C48-1
0.1
C52-1
100uF
C56-1
0.1
U30-1
LD1117S
ADJ
R96-1
120
R99-1
120
C65-1
10uF
C70-1
0.1
+2,5VLMS
L9-1
TI160808U601
C49-1
0.1
C53-1
100uF
C57-1
0.1
U31-1
LD1117S
R97-1
56
R100-1
120
C66-1
10uF
C71-1
0.1
+1,8VDLMS
L10-1
TI160808U601
C50-1
0.1
C54-1
100uF
C58-1
0.1
U32-1
LD1117S
R98-1
56
R101-1
120
C169-1
330uF
C72-1
0.1
+1,8VALMS
R110-1
51
R111-1
51
R112-1
51
R113-1
51
X16-1
RX_I
X17-1
RX_Q
C82-1
470p
R109-1
820
C83-1
8n2
R108-1
12k
C84-1
150p
C98-1
470p
R119-1
1k2
C97-1
150p
C99-1
8n2
R121-1
820
R114-1
6k8
R107-1
390
C85-1
0.1
X14-1
TST3
TXINIP
TXININ
TXINQP
TXINQN
TXCPOUT
TXVTUNE
XRES12k
XRESAD
VREFAD
AUXIN/ATPOUT
RXOUTIP
RXOUTIN
RXOUTQP
RXOUTQN
RXCPOUT
RXVTUNE
UNUSED
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UmTRXv2_DBG_20dBm_TCXO
Size
A3
Number
Revision
1
Date:
05.06.2012
Sheet 3 of 8
File:
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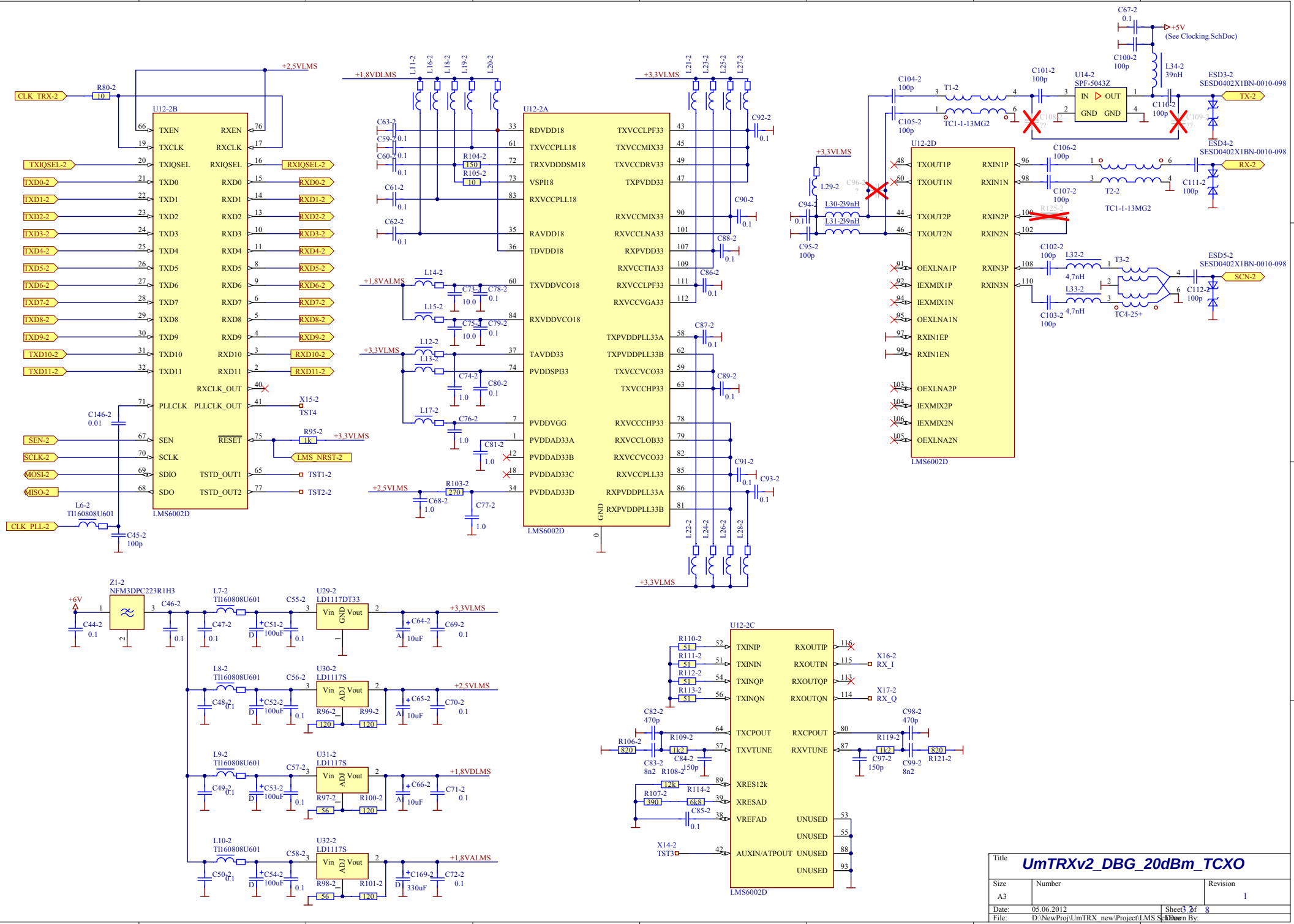

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Size: A3	Number	Revision: 1
Date: 05.06.2012	Sheet 3 of 8	
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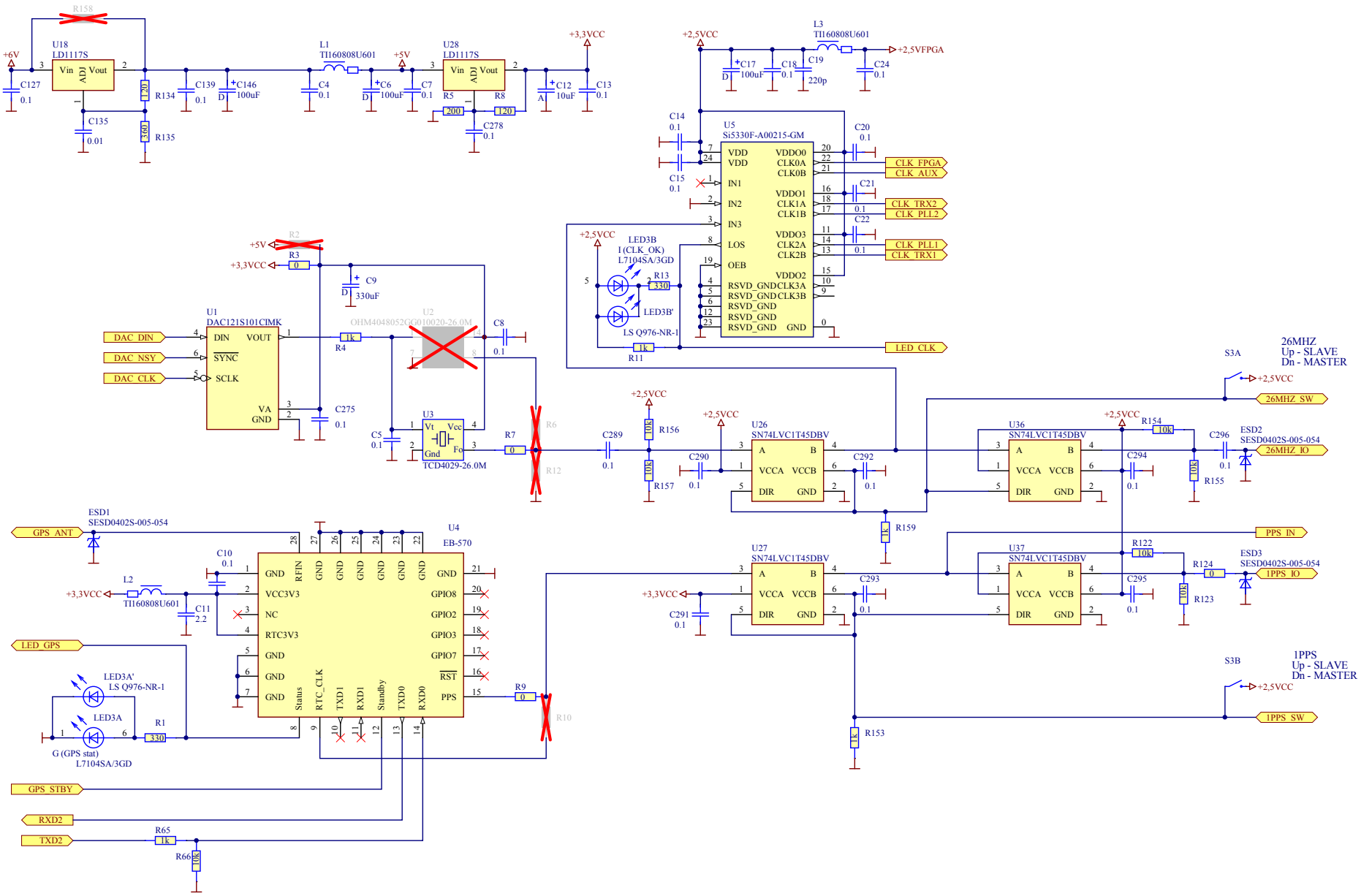

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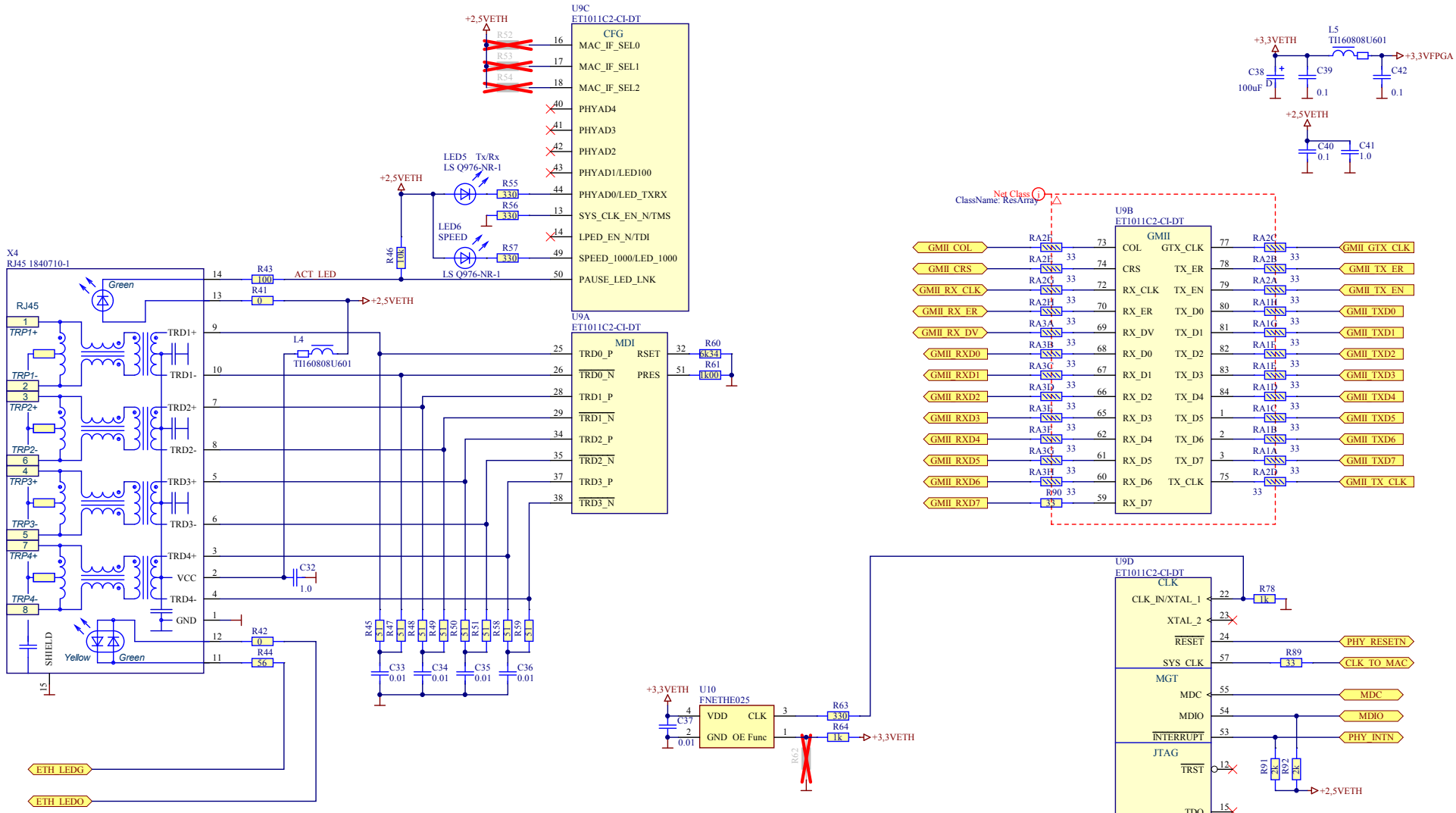
Size: A3	Number	Revision: 1
Date: 05.06.2012	Sheet 5 of 8	
File: D:\NewProj\...\Clocking.SchDoc	Drawn By:	



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Size: A3	Number	Revision: 1
Date: 05.06.2012	Sheet 6 of 8	
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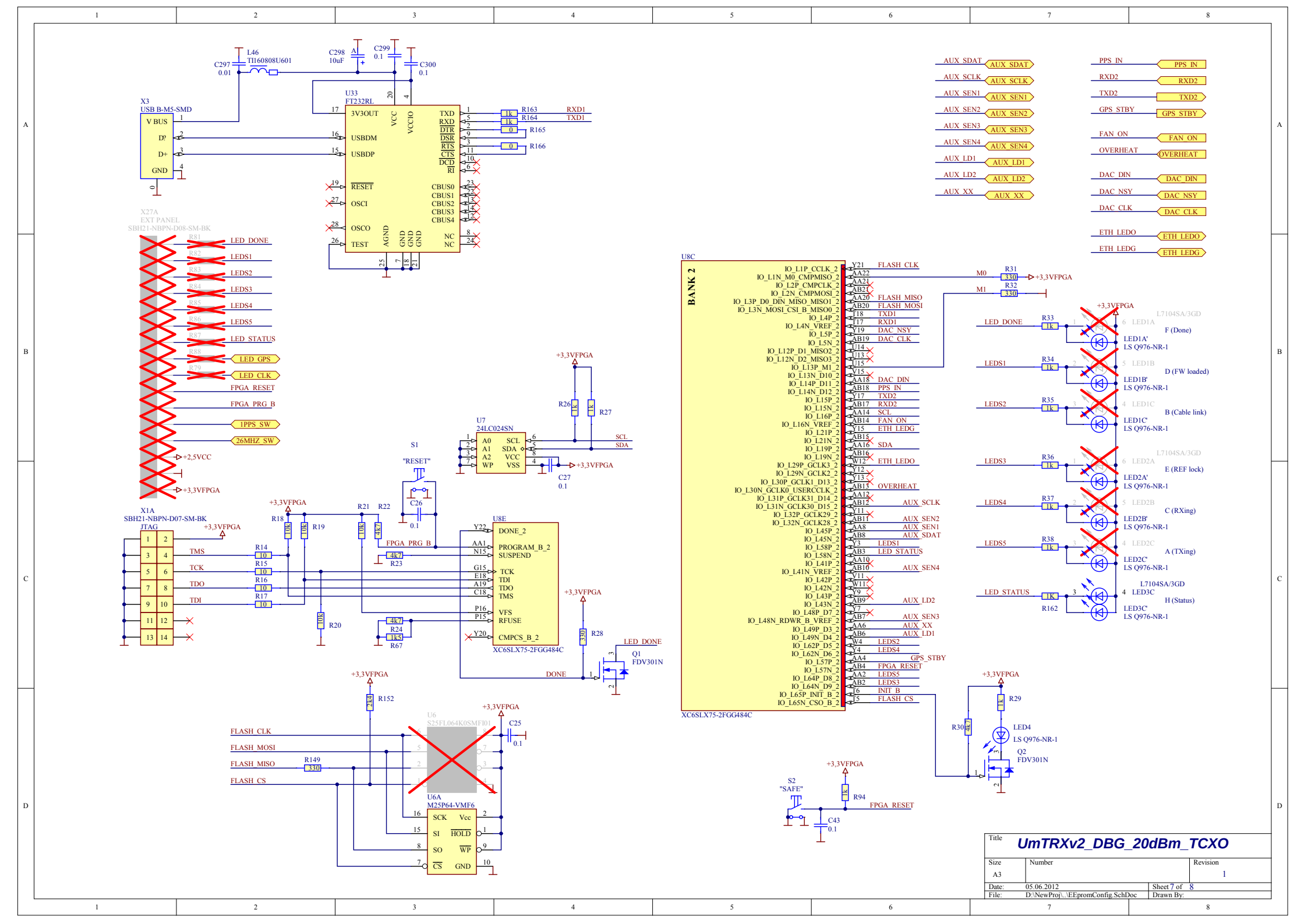
L46
TI160808U601
C297
0.01
C298
10uF
C299
0.1
C300
0.1
X3
USB B-M5-SMD
V BUS
D?
D+
GND
U33
FT232RL
3V3OUT
USBDM
USBDP
RESET
OSCI
OSCO
TEST
VCC
VCCIO
AGND
GND
TXD
RXD
DTR
DSR
RTS
CTS
DCD
RI
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
NC
R163
R164
R165
R166
RXD1
TXD1
X27A
EXT PANEL
SBH21-NBPN-D08-SM-BK
LED_DONE
LEDS1
LEDS2
LEDS3
LEDS4
LEDS5
LED_STATUS
LED_GPS
LED_CLK
FPGA_RESET
FPGA_PRG_B
1PPS_SW
26MHZ_SW
+2,5VCC
+3,3VFPGA
U7
24LC024SN
A0
A1
A2
WP
SCL
SDA
VCC
VSS
R26
R27
C27
0.1
S1
"RESET"
C26
0.1
X1A
SBH21-NBPN-D07-SM-BK
JTAG
TMS
TCK
TDO
TDI
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R67
FPGA_PRG_B
U8E
DONE_2
PROGRAM_B_2
SUSPEND
TCK
TDI
TDO
TMS
VFS
RFUSE
CMPCS_B_2
XC6SLX75-2FGG484C
R28
Q1
FDV301N
LED_DONE
DONE
U6
S25FL064K0SMFI01
U6A
M25P64-VMF6
SCK
SI
SO
CS
Vcc
HOLD
WP
GND
FLASH_CLK
FLASH_MOSI
FLASH_MISO
FLASH_CS
R149
R152
C25
0.1
U8C
BANK 2
XC6SLX75-2FGG484C
FLASH_CLK
FLASH_MISO
FLASH_MOSI
TXD1
RXD1
DAC_NSY
DAC_CLK
DAC_DIN
PPS_IN
TXD2
SCL
FAN_ON
ETH_LEDG
SDA
ETH_LEDO
OVERHEAT
AUX_SCLK
AUX_SEN2
AUX_SEN1
AUX_SDAT
LEDS1
AUX_SEN4
GPS_STBY
FPGA_RESET
LEDS5
LEDS3
INIT_B
FLASH_CS
AUX_XX
AUX_LD2
LEDS2
LEDS4
M0
M1
R31
R32
R33
R34
R35
R36
R37
R38
R162
LED1A
LED1B
LED1C
LED2A
LED2B
LED2C
LED3C
L7104SA/3GD
F (Done)
D (FW loaded)
B (Cable link)
E (REF lock)
C (RXing)
A (TXing)
H (Status)
LED1A'
LED1B'
LED1C'
LED2A'
LED2B'
LED2C'
LED3C'
LS Q976-NR-1
R29
R30
LED4
Q2
S2
"SAFE"
R94
C43
0.1
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UmTRXv2_DBG_20dBm_TCXO
Size
A3
Number
Revision
1
Date:
05.06.2012
Sheet 7 of 8
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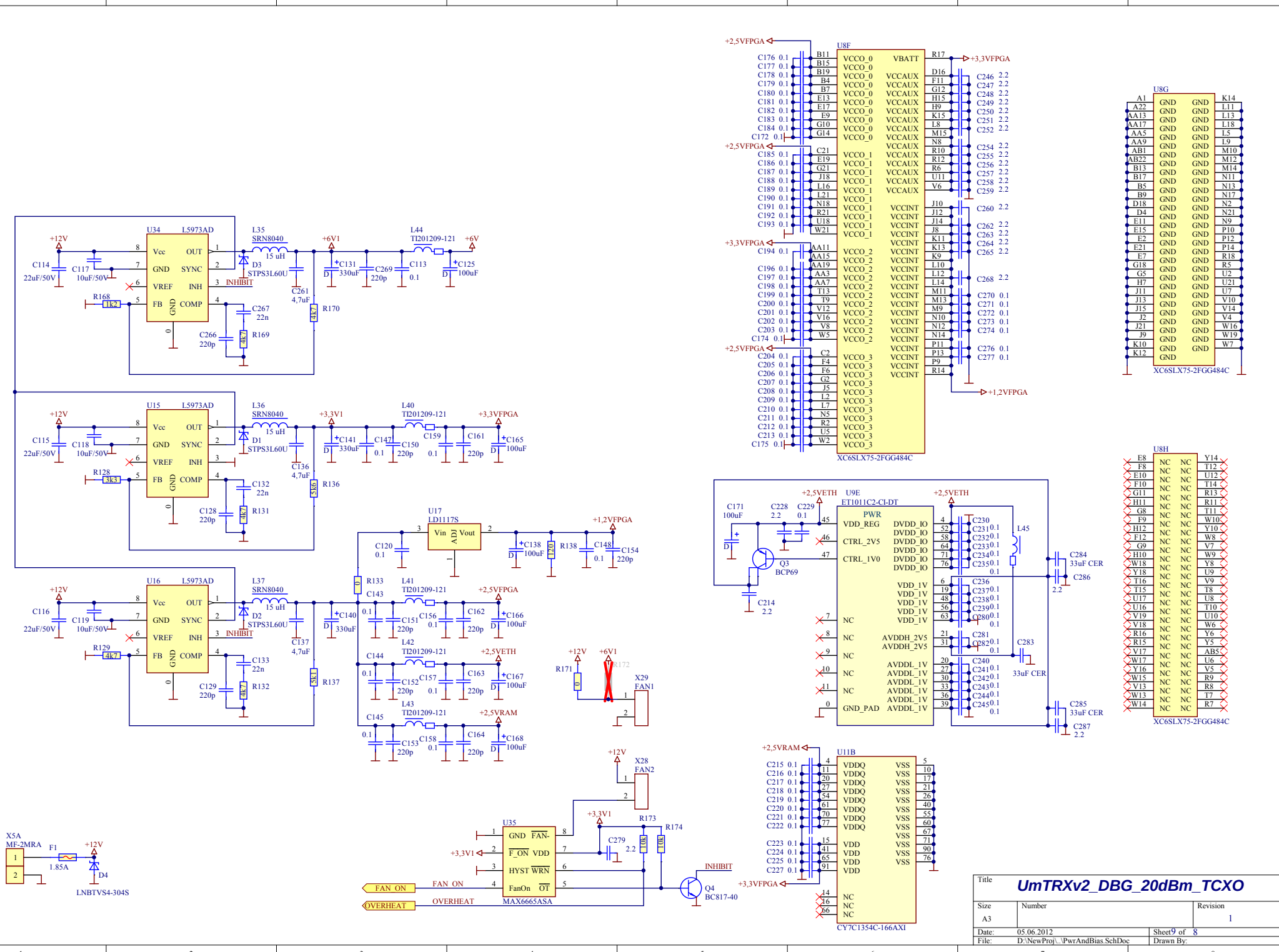
U8F
XC6SLX75-2FGG484C
U8G
XC6SLX75-2FGG484C
U8H
XC6SLX75-2FGG484C
U34 L5973AD
U15 L5973AD
U16 L5973AD
U17 LD1117S
U9E ET1011C2-CI-DT
U11B CY7C1354C-166AXI
U35 MAX6665ASA
X5A MF-2MRA
X29 FAN1
X28 FAN2
Q3 BCP69
Q4 BC817-40
D4 LNBTVS4-304S
FAN_ON
OVERHEAT
INHIBIT
+12V
+6V1
+3,3V1
+2,5VFPGA
+3,3VFPGA
+1,2VFPGA
+2,5VETH
+2,5VRAM
+6V
Title
UmTRXv2_DBG_20dBm_TCXO
Size
A3
Number
Revision
1
Date: 05.06.2012
Sheet 9 of 8
File: D:\NewProj\..\PwrAndBias.SchDoc
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