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LMS6002D Quick Start Manual

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Introduction

The EVB6002-5 is a general purpose evaluation board intended to allow evaluation and testing of the LMS6002D multi-band, multi-standard RFIC transceiver. It is not intended to act as a guide to the best layout, decoupling and matching practices when implementing the LMS6002D. The Lime LMS6002D reference board was developed with best layout, decoupling and matching practices to deliver optimum LMS6002D RF performance.

This document provides instructions on how to load the evaluation board software ctr6002d onto a PC, connect the PC to the board, control the LMS6002 via the ctr6002d software and evaluate its performance. A summary of the main steps to complete this is shown below:

- Install PC ctr6002d software.
- Connect power supplies and cables to the evaluation board.
- Turn on and do SPI and register checks.

Continue using this document to do the following:

- Hardware/Board system set up for integration with baseband platforms.
- Evaluate the LMS6002D performance.

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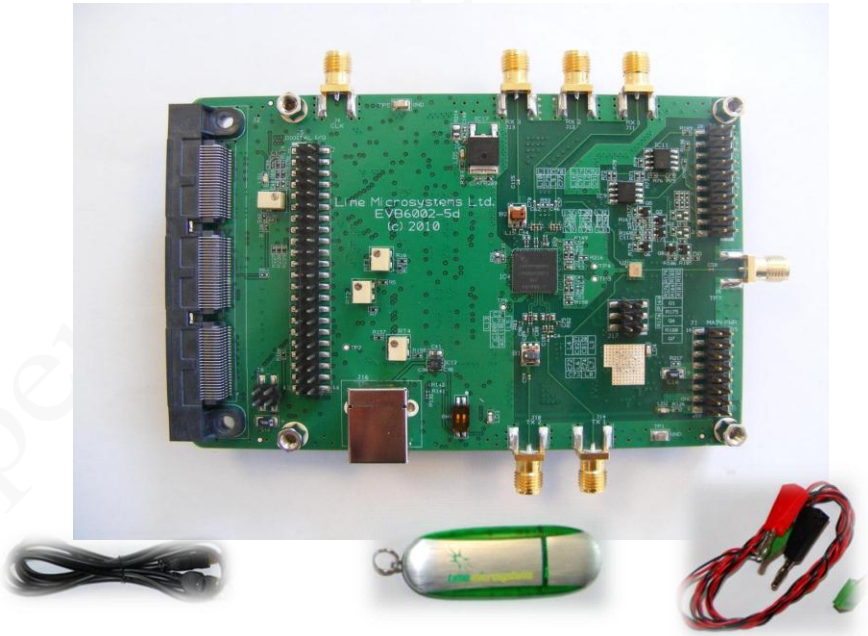
Development System Contents

Before commencing any work please ensure all of the contents listed below are contained in the system shipped. See Figure 1 Development System Contents below:



PC to USB cable | USB software stick | 5V Supply cable for LMS6002D Board

Figure 1 Development System Contents

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Evaluation Board Connections

The following chapter describes in detail EVB connectors, various SPI and clocking options.

3.1 Basic Connections

The analogue differential IQ BB interfaces are connected to transmit and receive paths via the J3 connector for use with test equipment. In addition there are on board differential to single ended drivers on each of the receiver outputs to accommodate testing with an oscilloscope. An interface via pin header J5 is provided to the parallel digital interface on the LMS6002D. A baseband connector via pin header J2 is also provided to be used with third party basebands.

RX IN 1 is tuned from 700 – 1500 MHz to cover UMTS bands V and VIII, whilst RX IN 2 is tuned from 1.5 – 2.5 GHz to cover UMTS bands I, II and III. RX IN 3 is connected with a broad band balun that enables it to cover all bands and require no matching. TX OUT 1 is optimized for band I, II operation while TX OUT 2 is tuned for broadband operation by the selection of the matching components.

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3.2 Board Connections

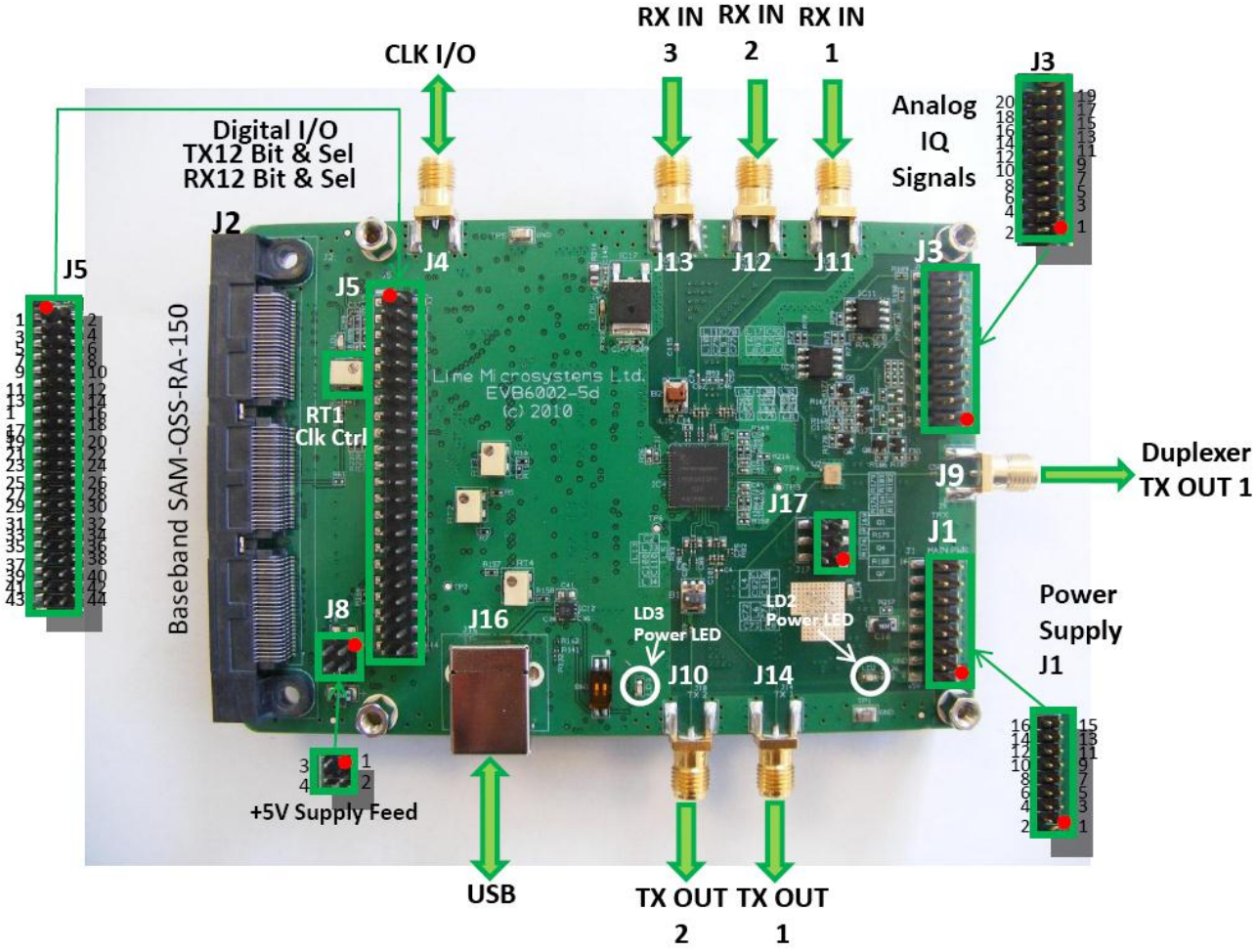

Figure 2 Evaluation board connection descriptions.

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The following table describes the high level pin assignment for each connector on the evaluation board.

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Connector	Name	Description
J1	5V Power Supply	5V supply feed used for standalone operation (not connected to baseband board). The board is shipped in this mode. To run the Lime boards using the power supply from a baseband card connect the links on connector J8 (see connector J8 for details).
J2	Baseband Board Connector	The SAM-QSS-RA-150 is a standard connector used to interface the Lime board directly to a base band board. Please note: Specific configuration settings, using 0 Ω resistors on the Lime evaluation board may need to be changed before connection to a baseband board, see section 3.5.
J3	Analogue IQ Signals	Analogue IQ signals can be used via this connector. Using the board in analogue device mode means the baseband TX and RX signals are connected via this connector. Using the board in digital device mode, this connector can be used as a test point to test the ADC & DAC's, analogue section of the transceiver or purely as a test point to monitor the signal in full operation mode. The transmit input signals required are differential I and Q. The Receiver signals have both single ended and differential outputs. Single ended provided for test purposes.
J4	CLK I/O	Clock input for locking the external clock from test equipment to the Lime on board clock. J4 connector is used to supply the on board ADF4002 board clock PLL device with 10 MHz clock, to lock the EVB reference clock with the measurement setup. Also, J4 can be used as output or as external reference clock from the LMS6002D.
J5	Digital I/O TX 12 Bit & Select and RX 12 Bit & Select	Connector used in standalone mode to input digitally 12 bit MUXED IQ signal into the transmit chain and receive digitally 12 bit MUXED IQ signal from the Receiver. Please refer to Lime LMS6002D data sheet for signal information.
J8	Baseband Supply Feed	Connector used to route power supply connections for use in standalone mode or using the power supplied from the baseband board via connector J2. Please refer to section 3.3.5 for details on configuration settings.
J9	TRX	Duplexer transmitter output 1 connection.
J10	TX OUT 2	Transmitter output TX2, output direct from the chip.
J11	RX IN 1	Receiver input RX1, input direct to chip.
J12	RX IN 2	Receiver input RX2, input direct to chip.

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J13	RX IN 3	Receiver input RX3, input direct to chip.
J14	TX OUT 1	Transmitter output TX1, output direct from the chip.
J16	USB	USB Connector to PC.

Table 1 Evaluation board connectors

3.2.1. J1 – Main Power Supply Connector

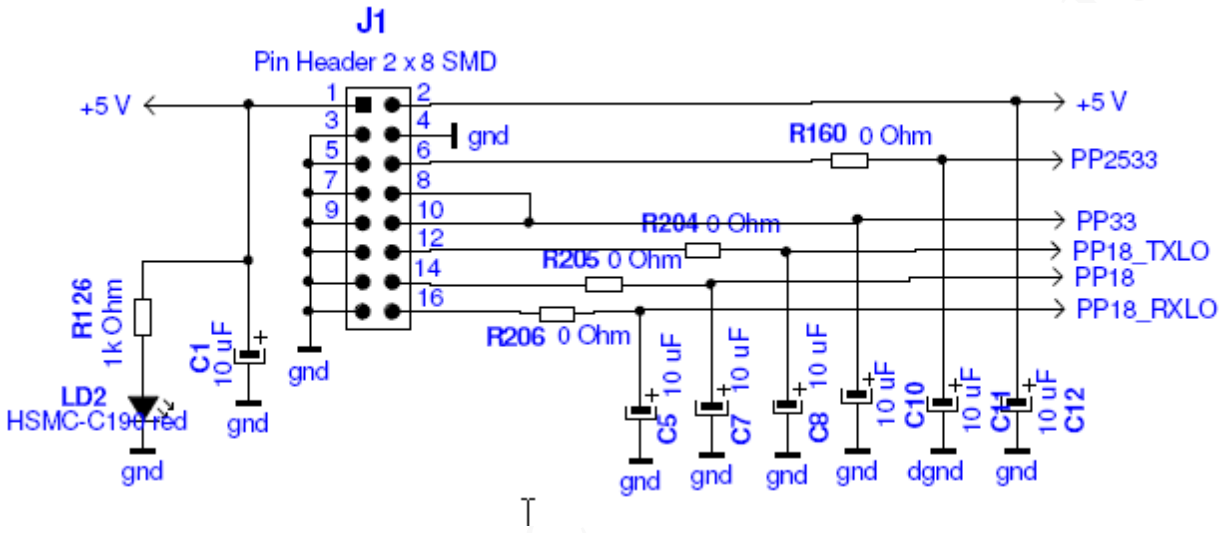
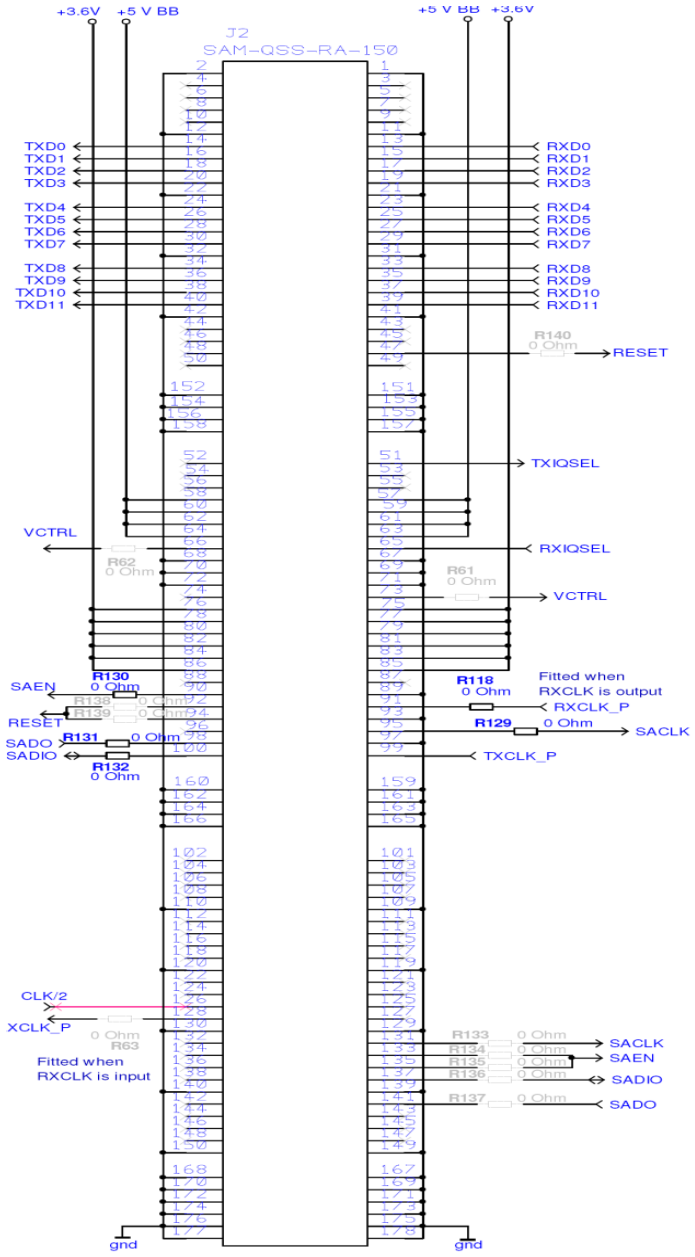


Figure 3 Connector J1 circuit diagram.

For standard mode Pin1 or Pin2 is connected to external power supply up to +5V. Pin 3 or Pin4 is connected to ground.

3.2.2. J2 – Third Party Baseband Board Connector

The SAM-QSS-RA-150 is a standard connector used by third party baseband providers.



The SAM-QSS-RA-150 is a standard connector used by third party baseband providers.

The LMS6002D board is shipped configured to operate using the connector J5 in standalone mode. The board has been fitted with several 0 Ω resistors which act as links to configure the board in different ways depending on which baseband board is being used.

Figure 4 Connector J2 circuit diagram.

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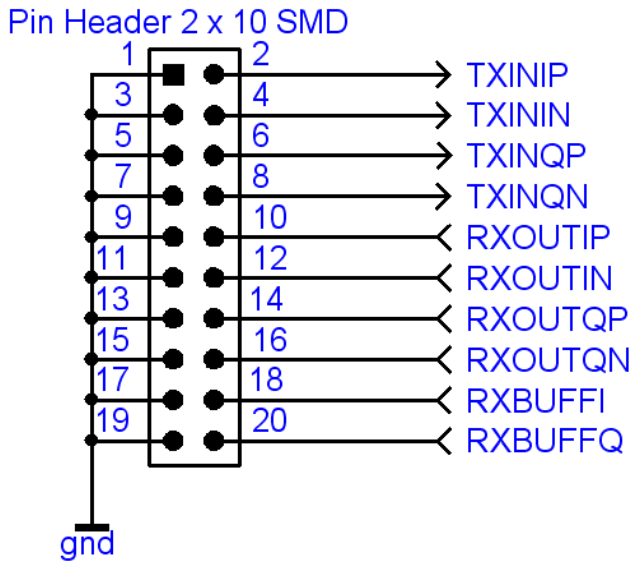
3.2.3. J3 – Analogue IQ Signals



Pins 18 and 20 of J3 connector are single ended analogue receiver outputs.

Pins 10, 12, 14 and 16 are differential analogue receiver outputs.

Pins 2, 4, 6 and 8 are differential analogue transmitter inputs.

All other pins are ground connections.

Figure 5 Connector J3 circuit diagram

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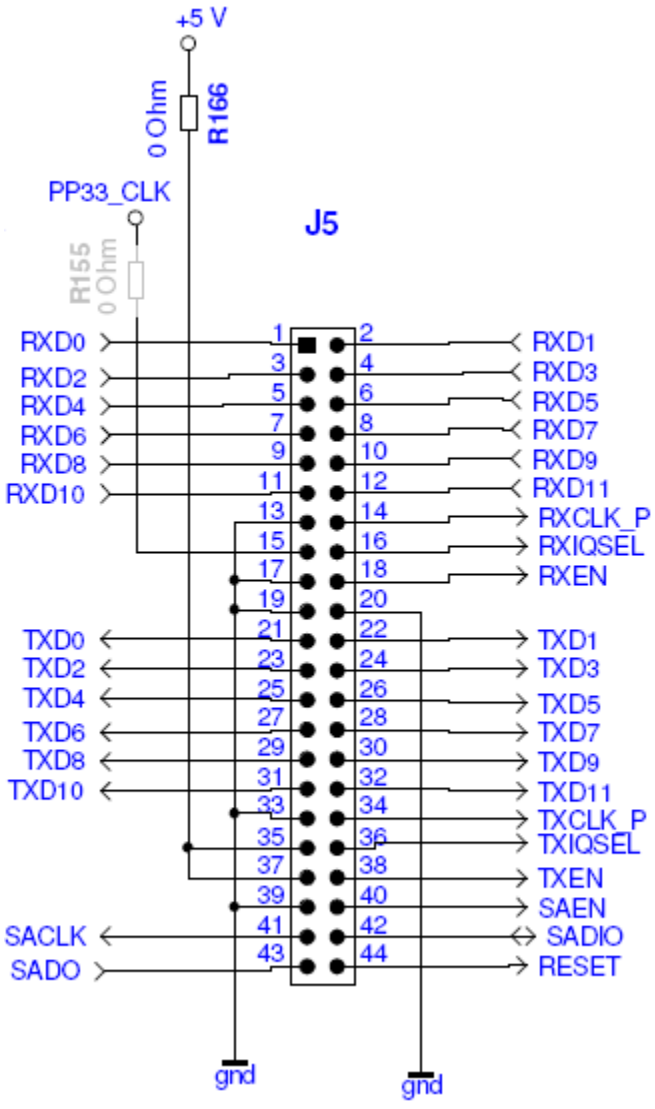
3.2.4. J5 – Digital I/O (I&Q) TX 12 Bit & TXIQSel and RX 12 Bit & RXIQSel



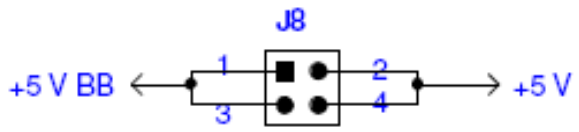
The digital I/Q connector is a digital transmit (TX) and receive (RX) interface to the ADC/DAC of the LMS6002D.

The SPI can be controlled within the J5 connector.

J5 can also be used as a test connector when the board is connected to a third party baseband board.

Figure 6 Connector J5 circuit diagram.

3.2.5. J8 – Sourcing 5V Supply from Baseband Board



J8 is used to power up board from baseband platform. Use jumper to power it up as shown by connecting pins 1 & 2 and/or pins 3 & 4.

Figure 7 Connector J8 circuit diagram

3.2.6. J16 – USB Connector

A type B USB connector is used to connect the PC to the evaluation board. It enables the LMS6002D to be programmed via the 6002Dr2 test GUI software that comes with the Quick Starter kit.

3.3 Hardware options: Clocking, TCXO & SPI.

This section describes the configurations and set up procedures for:

- TCXO frequency and data clocks distribution (Section 3.4).
- TCXO Locking method (Section 3.6)
- SPI connection options (Section 3.7).

The default mode the board is shipped with means basic operation using an external digital I/O source via connector J5 (digital I/O (I&Q) TX 12 Bit & Select and RX 12 Bit & Select). Various options are available depending on the system configuration required for testing or development work. The options are summarized below and the following sections will describe the board modifications required to achieve these configurations. Please note these are hardware options which are implemented via the following:

- Specific components to be fitted or not fitted.

3.4 TCXO Frequency and Data Clocks Distribution

The LMS6002D device provides a flexible clocking scheme which enables the PLL clock, RX clock and TX clock to be independently clocked.

The LMS6002D board is shipped with a default mode using the on board 30.72MHz clock provided. The board can be reconfigured to allow users to provide clocking from external devices using the two connectors J2 & J5. The most popular configurations are listed in the table below.

Option 1	DIO default mode	Description
PLL clock	30.72MHz TCXO	LMS6002D device PLL is fed using on board 30.72MHz TCXO.
Rx data clock	30.72MHz output	RX data clock is provided by Lime evaluation board and is fed to connectors J2 & J5 as outputs to enable a digital I/O card to capture samples.
Tx data clock	30.72MHz output	TX data clock is provided by Lime evaluation board and is fed to connectors J2 & J5 as outputs to enable a digital I/O card to send samples.

Option 2		Description
PLL clock	30.72MHz (TCXO ÷ 2)	LMS6002D device PLL is fed using on board TCXO 61.44MHz clock ÷ 2.
Rx data clock	61.44MHz output	RX data clock is provided by Lime evaluation board and is fed to connectors J2 & J5 as outputs to enable a digital I/O card to capture samples.
Tx data clock	30.72MHz output (TCXO ÷ 2)	TX data clock is provided by Lime evaluation board and is fed to connectors J2 & J5 as outputs to enable a digital I/O card to send samples.

Option 3		Description
PLL clock	30.72MHz TCXO	LMS6002D device PLL is fed using on board 30.72MHz TCXO.
Rx data clock	30.72MHz output	RX data clock is provided by digital I/O card and is fed to connectors J2 & J5 as inputs to enable Lime evaluation board to capture samples.
Tx data clock	30.72MHz output	TX data clock is provided by digital I/O card and is fed to connectors J2 & J5 as inputs to enable Lime evaluation board to send samples.

Table 2 Baseband Clock Configurations

The board is shipped in the default mode (Option 1). To use other options please make sure that hardware changes were applied as in the table below. Please note that NF denotes component is not fitted.

3.5 Different Clocking Schemes

Different Clocking Schemes			
	Option 1	**Option 2**	**Option 3**
	DIO default mode		
PLL clock	30.72 MHz TCXO	30.72 MHz TCXO	30.72 MHz TCXO
Rx data clock	30.72 MHz output	61.44 MHz output	Input from digital I/O card
Tx data clock	30.72 MHz output	30.72 MHz output	Input from digital I/O card
Evaluation Board	**Component fit option 1**	**Component fit option 2**	**Component fit option 3**
R81	NF	NF	0R
R80	NF	0R	0R
R104	NF	NF	NF
R105	0R	0R	NF
R106	0R	NF	NF
R107	68R	NF	68R
R111	NF	0R	NF
R113	0R	0R	0R
R114	0R	NF	NF
R116	0R	0R	NF
R117	0R	0R	0R
R110	NF	0R	NF
R39	NF	NF	NF
R40	NF	NF	NF
R58	NF	NF	NF
U4	NF	NC7SV74	NF
R147	NF	0R	NF
R148	0R	0R	0R
X1	E5280LFT (30.72 MHz)	NF	E5280LFT (30.72)
X2	NF	E5405 (61.44)	NF

Table 3 Baseband Clocking Schemes

3.6 TCXO Locking Options

The LMS6002D board provides different options to lock the TCXO to base band or test systems.

The LMS6002D board provides three options for clock locking:

Option 1 – Lock using on board PLL device ADF4002. This is the default mode the board is shipped with to enable the board to be locked to test equipment using an external 10MHz clock provided by connector J4, acting as an input.

Option 2 – Manual potentiometer - RT1. RT1 shown in figure 8 allows the TCXO to be manually tuned by altering the on board potentiometer. J4 becomes an output for the reference clock.

Option 3 – External control via the baseband connector J2. Signal VCTRL provided by baseband board.

The board is shipped in the default mode (Option 1). To use other options please use component changes as in table below. Please note that NF denotes component is not fitted.

TCXO Locking method			
Options	Option 1) DEFAULT MODE On Board PLL Clock (ADF4002)	Option 2) Manual Potentiometer	Option 3) External VCTRL
Description / Component	Lock to 10MHz input from test equipment J4=10MHz ref in	Manual Vtune J4=TCXO out	Use external DC voltage (from BB J2 connector VCTRL) to control TCXO J4=TCXO out
R39	NF	0R	NF
R40	NF	NF	0R
R58	NF	NF	NF
R61	NF	NF	0R
R62	NF	NF	0R
R104	NF	0R	0R

Table 4 TCXO Locking Method

Components R39, R40 and R61 are located on the top of the interface board as shown in figure 8.

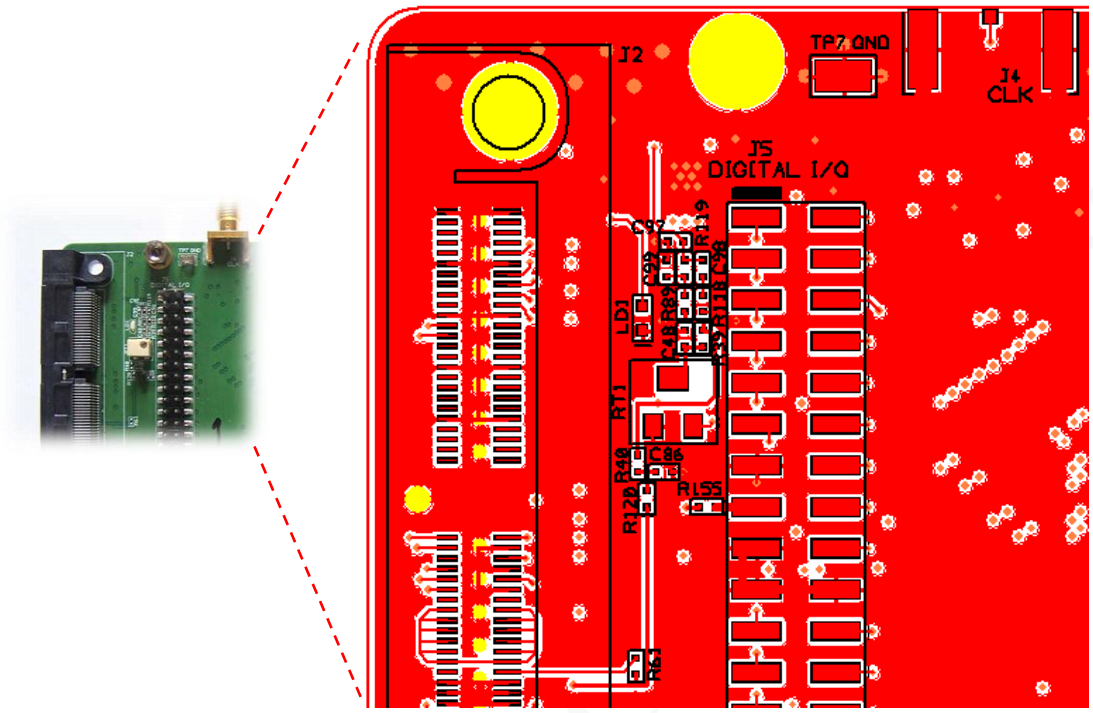


Figure 8 TXCO locking and SPI option components location (top side)

3.7 SPI Control Options

The LMS6002D board can be controlled by using the SPI connectors via J2, J6 or J16. Please note only one SPI master can be connected to the bus at any time, hence these are mutually exclusive.

The only option requiring hardware changes is Option 2 where the baseband connector J2 is used to connect to a baseband board (for the TX/RX signals) when its own SPI bus and control of the SPI by the Lime SW is desired (rather than the BB SPI). J2 must be removed from the EVB SPI bus so that the control of the SPI is maintained by a PC running the Lime software. This is required to ensure that the USB SPI connection via J16 does not conflict with the baseband SPI connections via J2. Please note that NF denotes component is not fitted.

SPI control		
Options	Option 1 DEFAULT MODE USB SPI via J16 or baseband board SPI via J2	Option 2 USB SPI control via J16 with J2 baseband SPI disabled. Used with 3rd party baseband boards and controlling LMS6002D with PC S/W via USB.
Description / Component	SPI connected to PC via USB connector J16.	SPI connected to BB via connector J2 SAMTEC
R133	NF	0R
R134	NF	0R
R135	NF	0R
R136	NF	0R
R137	NF	0R

Table 5 SPI Control Options

All of these components are located on the underside of the board and can be located using the diagram below.

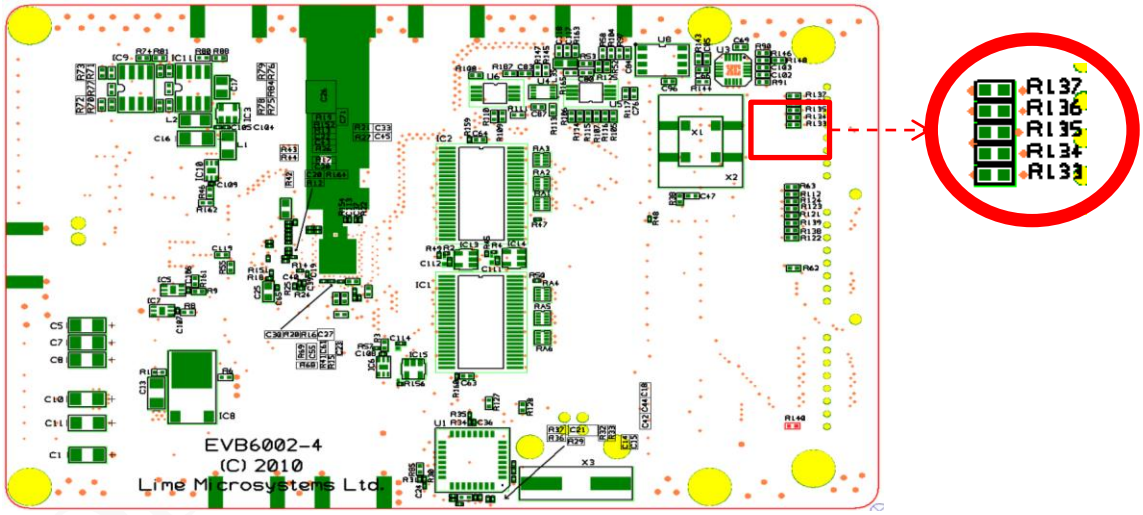


Figure 9 SPI control resistor component locations

4

Installing and Running PC Software Application

4.1 Windows XP Operating System

Plug USB cable to USB port of the interface board.

1. You will need to be logged in as Administrator to the free USB port on your Windows machine.

2. No external power connection is required.

After plugging in the board Windows' *New Hardware Wizard* should appear. After installation procedure begins, DO NOT let Windows search as it will not find anything.

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Figure 10 Hardware wizard.

Next, you will want to install from a specific location.

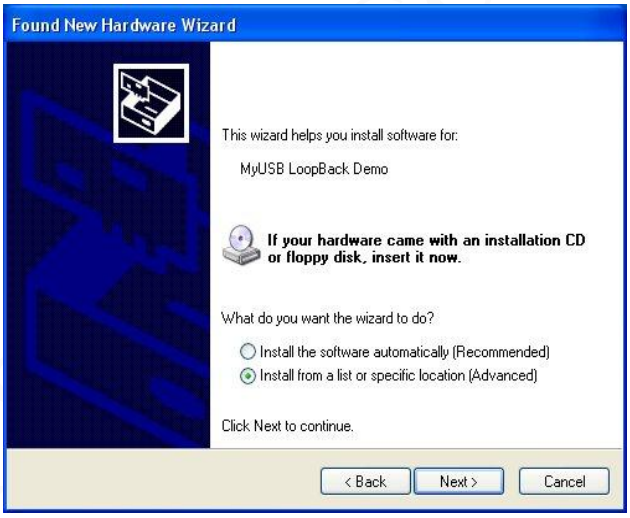

Figure 11 Hardware wizard. Install driver manually

Next, you need to point to the **`USBDriver.inf`** file, which can be found in the **QuickStarterKit** folder. Use the browse function to find this file. The same file for Windows XP and Windows Vista should work fine.

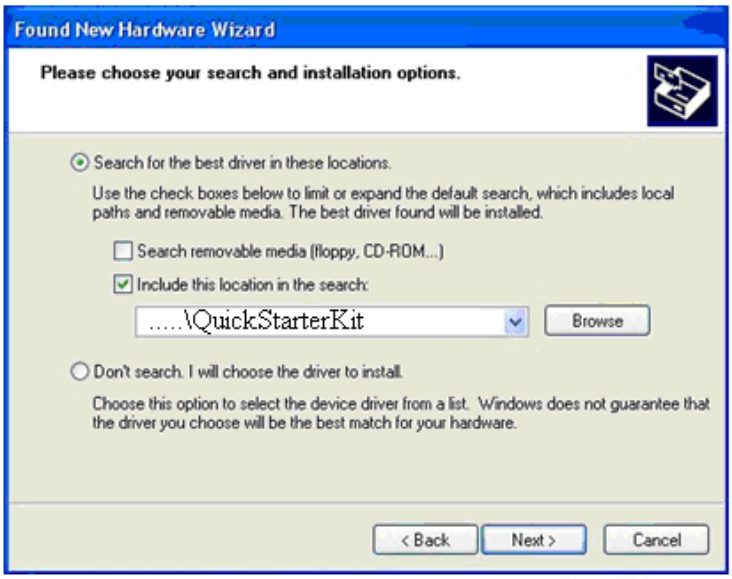

Figure 12 Hardware wizard. Choose the USBDriver.inf from the folder

Windows should proceed to install drivers. Enumeration process (USB term meaning *"connect and establish communication with"*) should start now. If everything is successful unplug and then plug in your device again to be able to use it.

4.2 Determining Serial Port

After enumeration (USB term meaning *"connect and establish communication with"*) Windows will assign to your USB Virtual Serial device a serial port - **COM?**.

Right-Click on **My Computer**, then click **Properties**, then the **Hardware** tab, then **Device Manager**, then find **USB Virtual Serial Port** under "Ports (COM & LPT)". Note that in this system example it has enumerated as COM3.

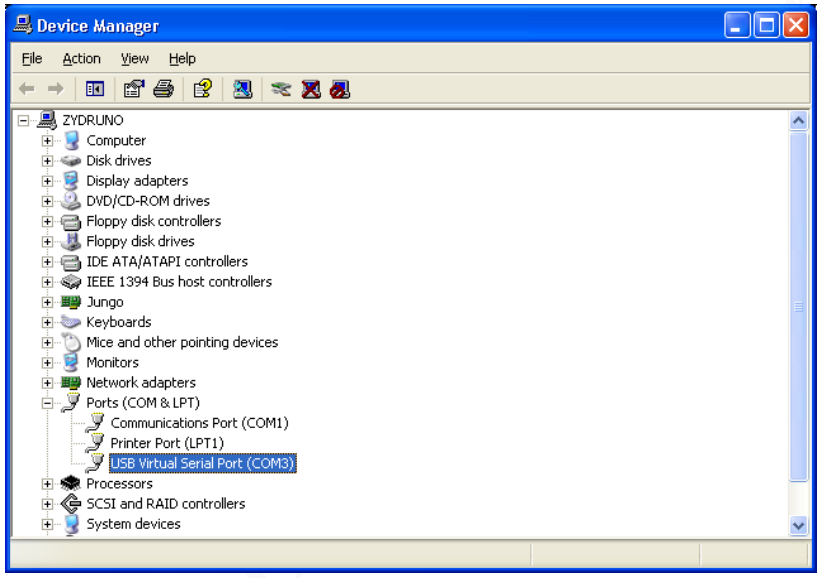

Figure 13 Check in device manager the new communication port

4.3 Windows 7 Operating System

Plug USB cable to USB port of the interface board. No external power connection is required.

After plugging in the board the USB driver needs to be installed. To install the USB driver do the following:

1. Click on Control Panel ⟶ System and Security ⟶ System.
2. Click on Device Manager ⟶ Other devices.
3. Right click on "LUFA USB-RS232 Demo" icon.
4. Click on Update Driver Software and select 2nd option: Browse my computer for driver software. Locate and install driver software manually as shown below.

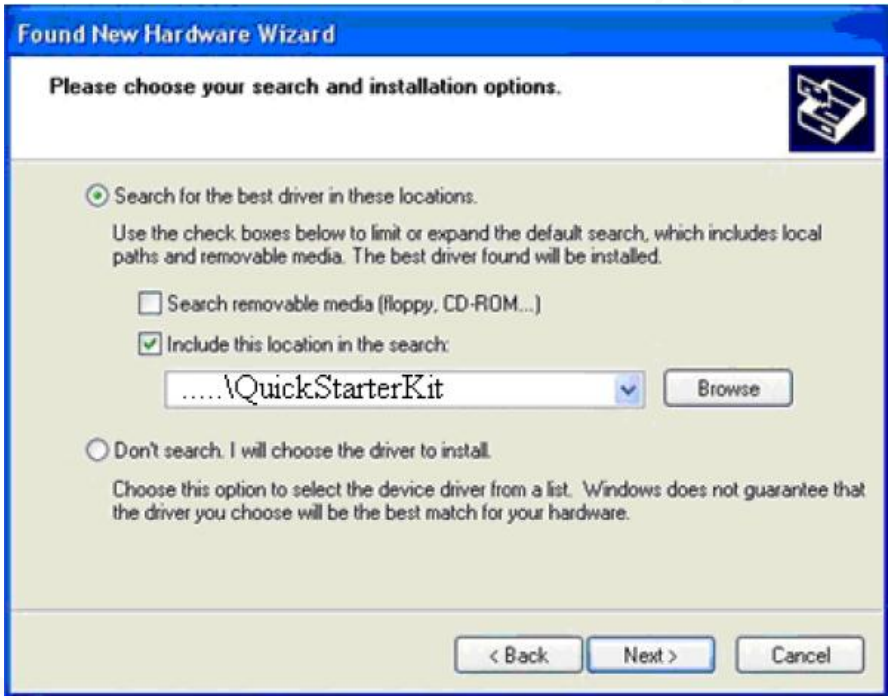

Figure 14 Device Manager. Choose the USBDriver.inf from the folder.

5. The folder should point to the `USBDriver.inf` file, which can be found in the **QuickStarterKit** folder. Use the browse function to find this file.
6. Windows should proceed to install drivers. Enumeration process (USB term meaning *"connect and establish communication with"*) should start now. If everything is successful unplug and then plug in your device again to be able to use it.

4.3.1. Determining Serial Port

After enumeration (USB term meaning *"connect and establish communication with"*) Windows will assign to your USB Virtual Serial device a serial port - **COM?**.

Click on **Control Panel**, then click **System and Security**, then click **System,** then click **Device Manager**, then find **USB Virtual Serial Port** under "Ports (COM & LPT)". Note that in this system example it has enumerated as COM4.

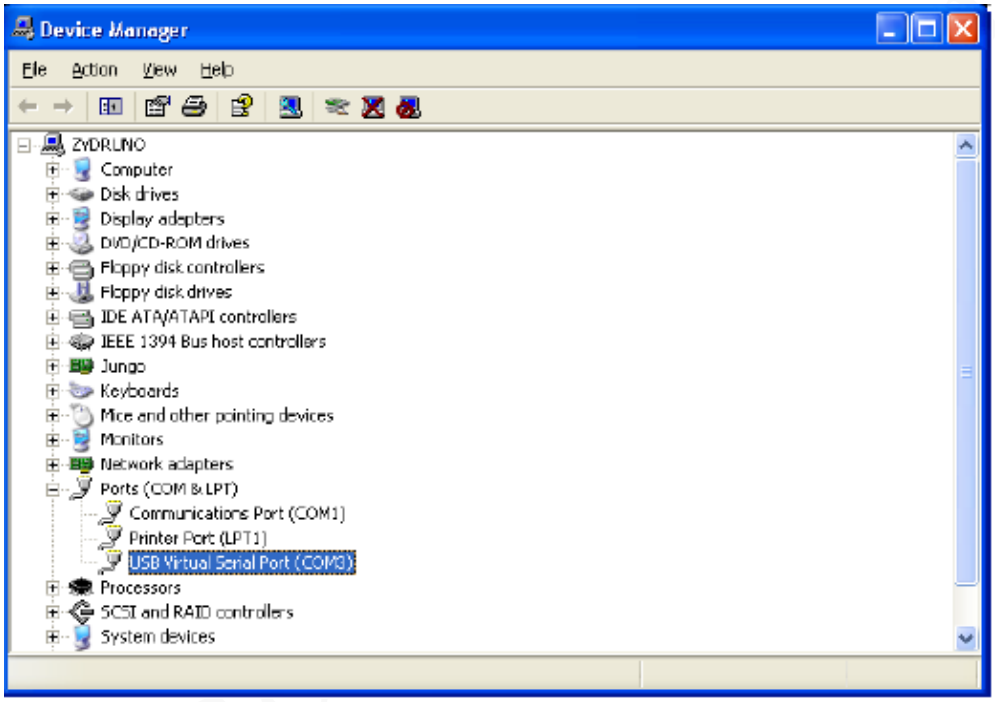

Figure 15 Check in device manager the new communication port.

4.4 Turn On and SPI Check

Turn on the +5V power supply to the board. The current should read approximately 0.15A on the power supply.

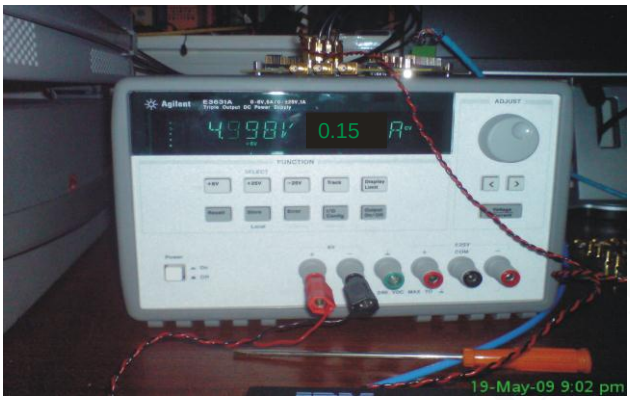

Figure 16 Power supply reading

Start LMS6002D board control S/W, located in QuickStarterKit transferred from the Lime USB stick. The SPI APP – picture of ICON is shown below.

Note: For Window 7 operating system, right click on the "ctr_6002dr2.exe" icon above. Next, click on Properties and click on the "Compatibility" tab as shown below.

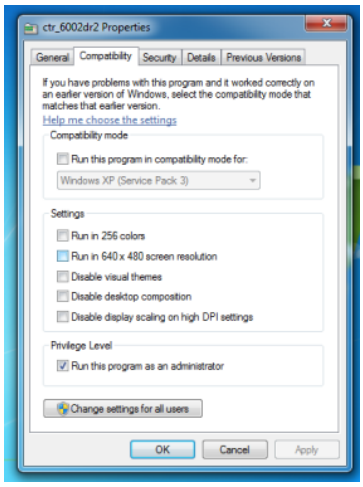

Figure 17 Run ctr_6002dr2 program as an administrator.

Select “Run this program as an administrator”. This will provide administrator privileges which is required for LMS6002 communication via USB.

Go to menu “Options->Communication Settings”. The following window appears.

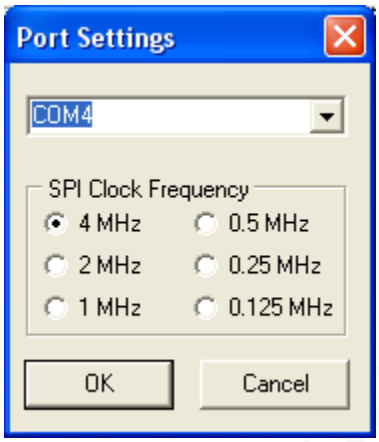

Figure 18 GUI communication settings.

Select enumerated port under USB board. In this case it is COM4 but port may be different Choose desired SPI clock frequency and push OK. Now you are able to communicate with the LMS6002D test board using USB to Serial adapter.

To check this is working select the register test sequence by going to menu “Tools->Register Test”.

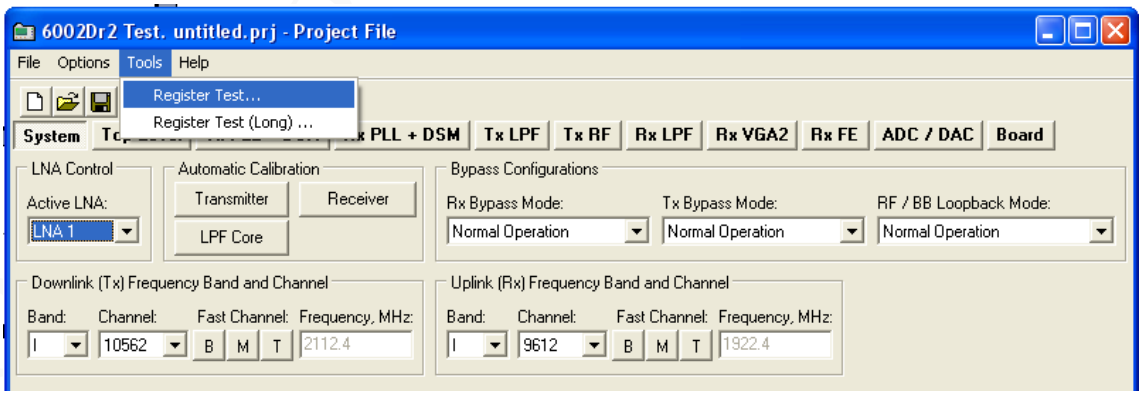

Figure 19 GUI register test.

The system will then return a full registers indicating OK for correct operation as shown below.

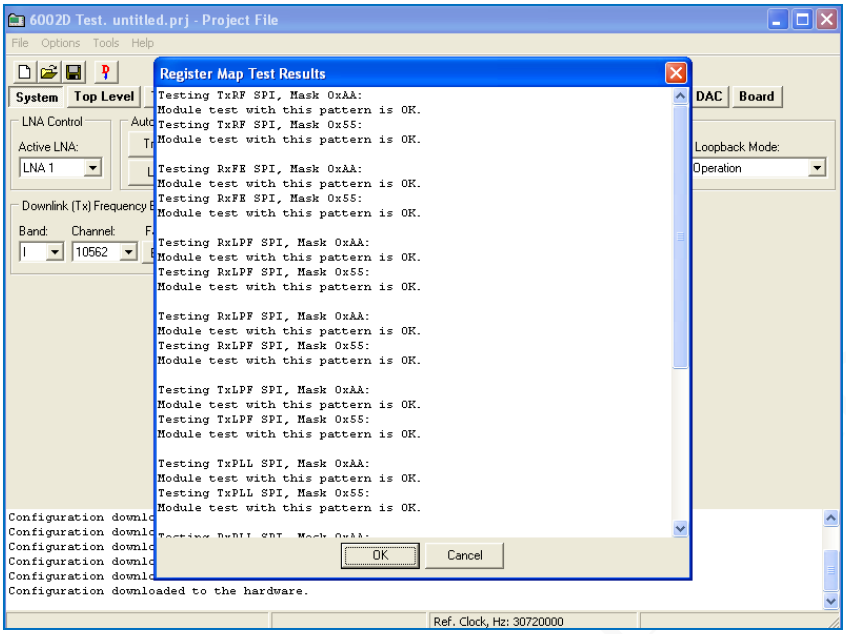

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Figure 20 GUI register test log.

If the system returns OK message you are now ready to commence testing. If the system returns 00 or FF instead of the OK this means there is a communication problem with the LMS6002D.

If the system test has returned 00 or FF instead of OK then shut down ctr_6002dr2 software and disconnect the Lime interface board. Leave for a few seconds before connecting the board and opening the ctr6002dr2 software again. Start registers test process again.

If the system returns 00 you know you have a problem with the connection between the PC and the evaluation board USB port. You will need to check connection and start the process again.

If the system test returns FF then you know the PC and the USB port are communicating properly. Connect the Lime board to +5V supply and start the process again. If you now get an OK for the register test map results then the system is ready for testing. If the system still returns 00 or FF instead of an OK, reboot entire connected system starting with the PC.

Note: When you close the software, the selected communication port and all of the associated settings will be saved under a file with *.CPS extension. Next time you run the software all the settings will be loaded automatically.

After the PC has finished rebooting apply power to the LMS6002D board and restart registers testing.

You should now see the correct OK message. The system is now ready to commence testing.

4.5 Ctr6002dr2 – Software Description

This section describes the ctr6002dr2 software tool and each of the buttons and embedded controls. Most of the pages in the tool can be read across to the top level sections of the SPI programming map, with the exception of the 'System page' and the 'Board' page.

4.5.1. System Interface

The System interface page allows configuring the synthesizers to the 3GPP bands by channel number and has buttons for bottom, middle and top frequencies for each. This makes changing frequency for the commonly used test channels simpler.

Automatic calibration (the calibrations the device carries out itself under SPI prompting) is also done from this page.

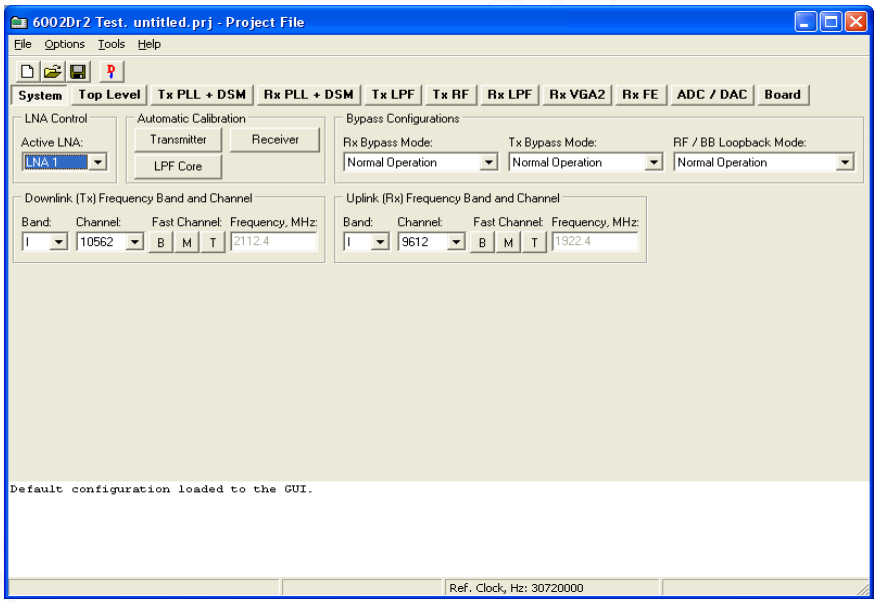

Figure 21 GUI System window.

Downlink and Uplink Frequency setting by band/channel number.
The synthesizers can be configured by channel number to the correct frequency in each 3GPP band. Buttons are provided for bottom, middle and top frequencies for each band. This makes changing frequency for the commonly used test channels easier.

Bypass configurations

The various bypass test modes and loop back test modes can be implemented by selecting from the drop down boxes, default is Normal operation.

Automatic Calibration

The Automatic calibration buttons can be used to run through the series of SPI commands required to implement the various self-calibration routines provided on the chip. Use of these macros is implemented as part of a calibration procedure and each button does not carry out a full calibration, use of the buttons in the wrong context could make the calibration state worse rather than better.

Automatic calibration should be done in the following order:

a. LPF Core – Press LPF core button

Executes the process related resistor capacitor (RC) calibration. LPF Core calibration is performed once per device to ensure that the corner frequencies of the LPFs are optimized. The calibration selects the LPF response which is closest and above the required bandwidth. This ensures modulation quality is not adversely impacted but sufficient rejection is provided for adjacent and alternate channel attenuation.

This should be done 1st as optimum DC calibration values for LPF's will change if this is done after the filter DC calibration.

b. Transmitter

The transmitter calibration executes a DC calibration on the TX LPF (I and Q) circuit. This makes the DC contribution at output of filters zero so that DC level at the mixer input does not change when the TX VGA1 gain is changed.

When executing this calibration make sure that no signal is applied to the transmit path. For better DC calibration low DC level signal can applied from baseband via DAC's to transmit path.

c. Receiver

Executes a DC calibration on the Rx LPF (I and Q), and Rx VGA2 (I and Q). This minimizes the DC contribution at output of filters and Rx VGA2.
When executing this calibration make sure that there is no signal applied to Rx input.

4.5.2. Top level

Various loop back and calibrations are also controlled on this page. They are not needed for basic operation. Automatic calibrations should all be done from the 'System' page where macros have been written to apply the calibration routines automatically.

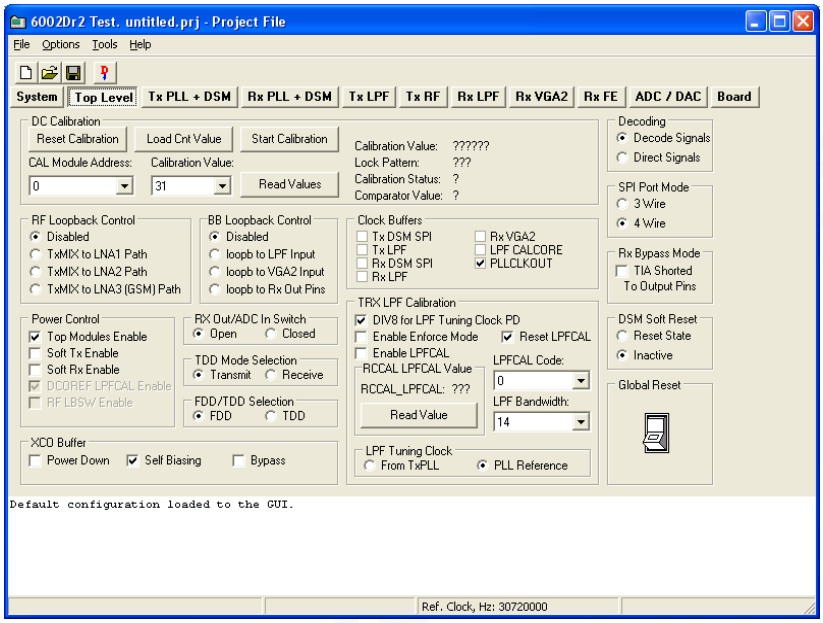

Figure 22 GUI Top Level window

Description of each function available from this page is as follows:

DC Calibration

Carries out the top level DC calibration for the device, this is the R component of the RC cal value which is used in each of the LPF (Tx and Rx) process calibration values. Only calibration module address 0 is used.

Clock Buffers control

Enable pins turn the internal clock buffers on and off. These should be enabled when control of the device is needed, however during operation SPI clocks which are not being used should be disabled to reduce the risk of SPI clock spurious.

RF Loopback Control

Test mode. RF loopback control sets the path used for the loopback from Tx to Rx input. Please refer to the SPI programming and calibration document for further details.

BB Loopback Control

Test modes, sets the BB loopback from Tx to Rx input.

Power Control
Soft turn off of Tx and Rx top level blocks of the LMS6002D via SPI. The LMS6002D communication can be easily checked by toggling the "Soft Tx Enable" and "Soft Rx Enable" in the Power Control section. The current change can be observed on power supply.

TRX LPF Calibration
This section is used to calibrate the capacitance of the device to ensure the LPF BW's are correct. To execute the calibration, check then uncheck the reset LPFCAL box (to reset calibration module). Then, check and uncheck the Enable LPFCAL box to execute the calibration. The result can be found in the DC calibration area when the read button is pressed.

Enable Enforce Mode and LPFCAL Code are not used. LPF BW sets the bandwidth used for the calibration. If you are using WCDMA select 2.5MHz. The result should be copied into the TXLPF and RXLPF from 'TRX_LPF_CAL' drop down box.

Decoding
Select 'Decode Signals' or 'Direct Signals' for control of different parts of the SPI memory map. Use 'Decode Signals'.

SPI Port Mode
Selects 3 or 4 wire SPI mode. 4 wire mode is used with the USB board solution.

Rx Bypass Mode
Not used.

DSM Soft Reset
Keep on inactive.

Global Reset
Toggles the reset pin via the USB SPI interface. The LMS6002D should be reset after power up to put it in a known state.

Rx Out/ADC In Switch
Select Closed to monitor receiver analog input. Select Open to route external signal to ADC.

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4.5.3. TX PLL + DSM

The Tx PLL is controlled from this page. If the frequency control on the 'System Interface' page is used and the correct 'set up files' have been automatically downloaded, then this page should not be needed. However a few points to check are that the tick boxes shown in the diagram below are enabled:

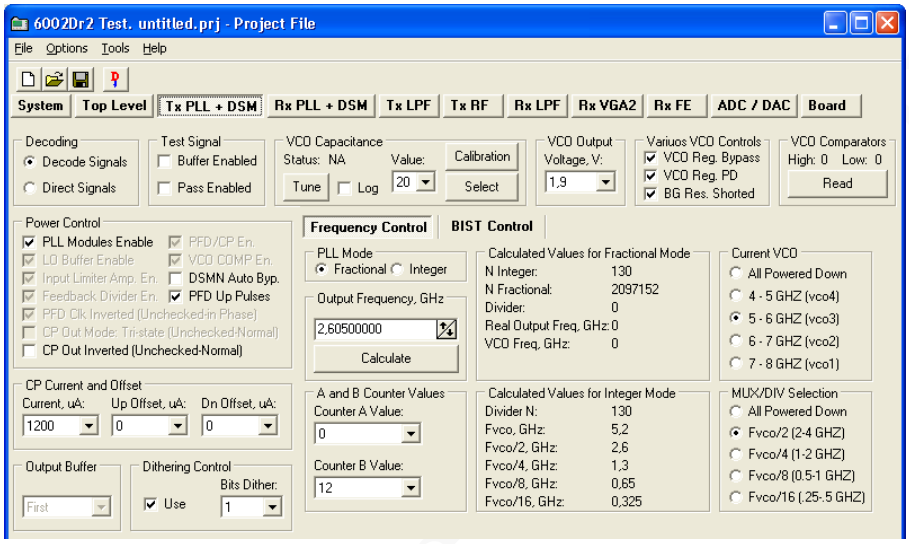

Figure 23 GUI TxPLL + DSM window

Description of each function available from this page is as follows:

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

Dithering Control
DSM dithering. Leave it set to 1.

Power Control
Individual parts of the PLL circuitry can be turned on and off – leave as default.

Test Signal
Design test signals – leave unchecked.

VCO Comparators
Reads the state of the VCO Comparators. Truth table is:

VTUNE_H	VTUNE_L	Status
0	0	ok
1	0	Vtune is high (> 2.5V) PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V) PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

Table 6 Comparator readings

Output Buffer
Control not used in TxPLL.

Frequency Control
Sets the PLL divide ratios, VCO and output divider selection. The individual parts of this block are described in more detail below:

PLL Mode – selects fractional or integer mode. Use fractional mode.

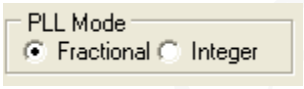

Figure 24 PLL mode.

Output Frequency (GHz) - set the desired Tx LO frequency in the text box.
'Calculate' button – calculates the required divide ratio based on the required LO frequency and reference frequency.

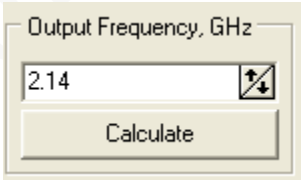

Figure 25 Output Frequency – GHz

These are shown in **'Calculated Values for Fractional Mode'** display box.

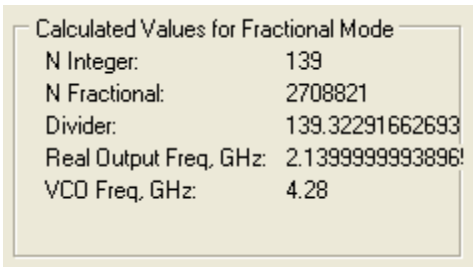

Figure 26 Calculated Values for Fractional Mode

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

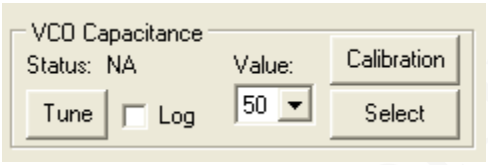

Figure 27 VCO Capacitance

The '**Current VCO**' and the '**MUX/DIV Selection**' show the choice made by pressing **"Calculate"** or **"Tune"** buttons, see below.

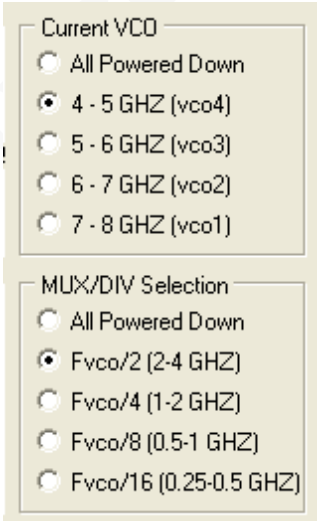

Figure 28 Current VCO and MUX/DIV selections

VCO Capacitance

Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide**.** Selections made when using the **'Calculate'** button however are decided based on the calibration table used in this block.

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

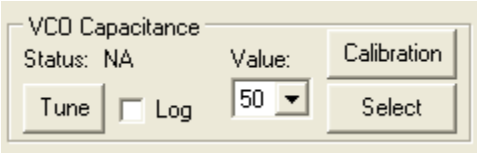

Figure 29 VCO Capacitance

Use of the **'Calibration'** button is described at the end of this section.

Charge Pump(CP) Current and Offset

Figure 30 CP Current and Offset

CP Current and Offset is set based on the selected loop filter and loop BW. For the recommended loop filter (implemented on the evaluation board) Current should be 1200uA and Up Offset 30uA, as shown.

PLL Calibration Data and File

Press the 'Calibration' button to enter the Frequency vs Capacitance calibration table data.

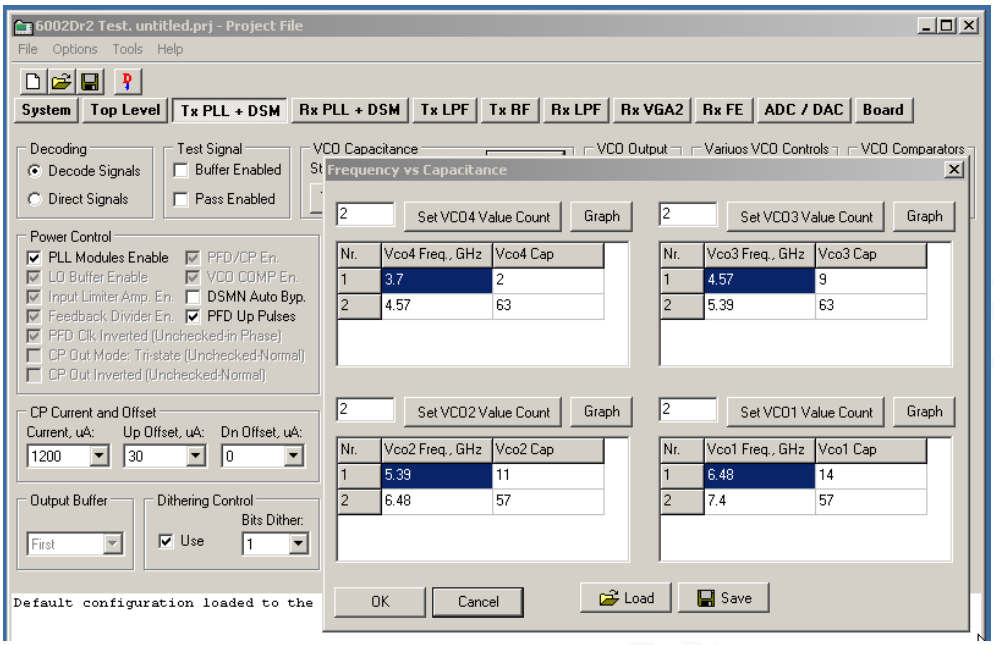

Figure 31 Frequency versus capacitance calibration table data

The calibration data consists of frequency versus capacitance value responses which are defined by minimum 2 point definition. The loaded VCO file should contain the above data. If not file 'Dr2.vco', provided with SW, should be loaded. To load a new VCO file press the 'Load' button and follow the normal windows procedure to load a file. Then press OK. This new file will now be downloaded on subsequent starts of the software.

4.5.4. Rx PLL + DSM

The Rx PLL is controlled from this page, if the frequency control on the 'System Interface' page is used and the correct 'set up files' have been automatically downloaded, then this page should not be needed. However a few points to check are that the tick boxes shown in the diagram below are enabled.

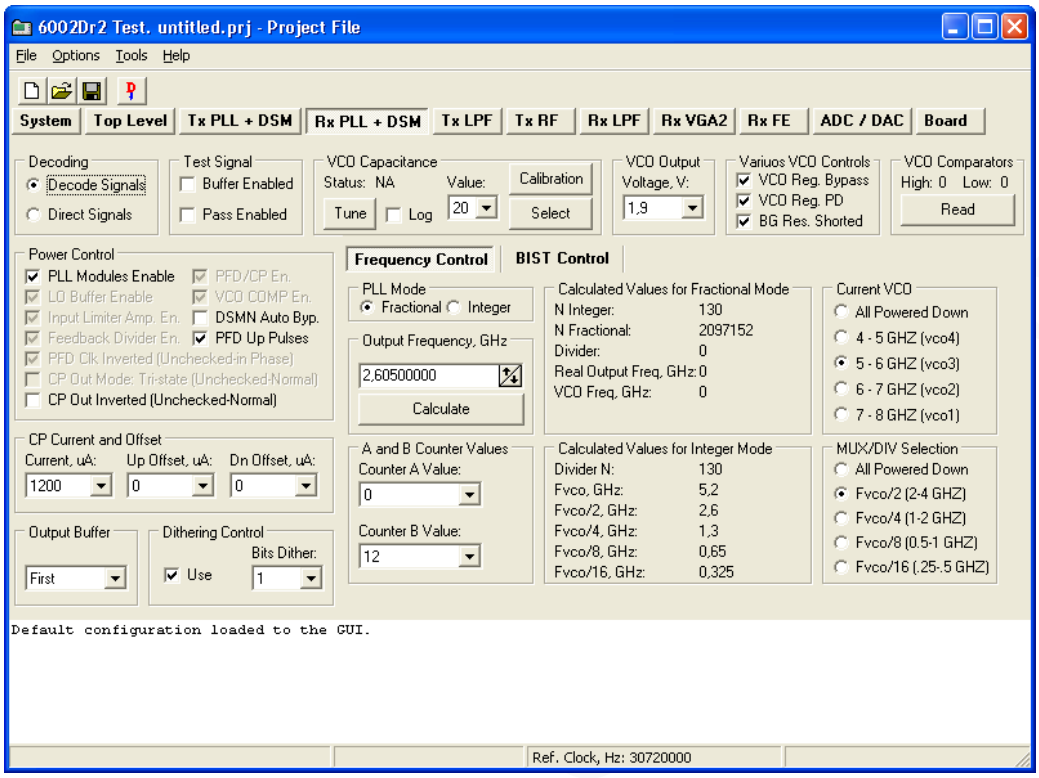

Figure 32 RX PLL + DSM page

Description of each function available from this page is as follows:

Decoding

Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

Dithering Control

DSM dithering. Leave it set to 1.

Power Control

Individual parts of the PLL circuitry can be turned on and off – leave as default.

Test Signal

Design test signals – leave unchecked.

VCO Comparators

Reads the state of the VCO Comparators. Truth table is:

VTUNE_H	VTUNE_L	Status
0	0	ok
1	0	Vtune is high (> 2.5V), PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V), PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

Table 7 Comparator readings

Output Buffer
Sets the correct PLL output buffer for the selected LNA:
LNA 1 = First
LNA 2 = Second
LNA 3 = Third and
Disable.

Selection of LNA in tool on 'System' page automatically selects the correct buffer.

Frequency Control
Sets the PLL divide ratios, VCO and output divider selection. The individual parts of this block are described in more detail below.

PLL Mode – selects fractional or integer mode. Use fractional mode.

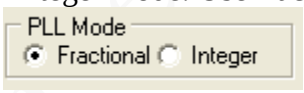

Figure 33 PLL Mode

Output Frequency (GHz) - set the desired Tx LO frequency in the text box.
'Calculate' button – calculates the required divide ratio based on the required LO frequency and reference frequency.

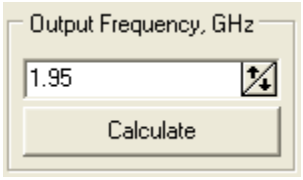

Figure 34 Setting receiver frequency - GHz

These are shown in **'Calculated Values for Fractional Mode'** display box

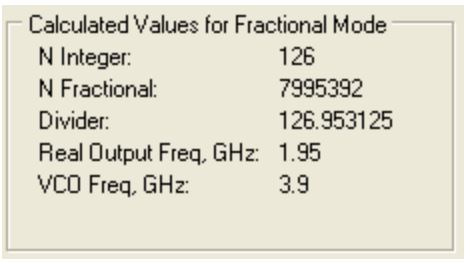

Figure 35 Calculated values for fractional mode

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

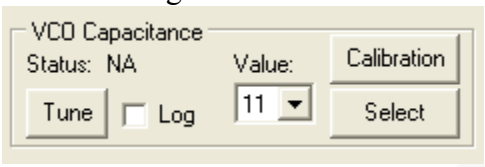

Figure 36 VCO Capacitance

The '**Current VCO**' and the '**MUX/DIV Selection**' show the choice made by pressing **"Calculate"** or **"Tune"** buttons, see below.

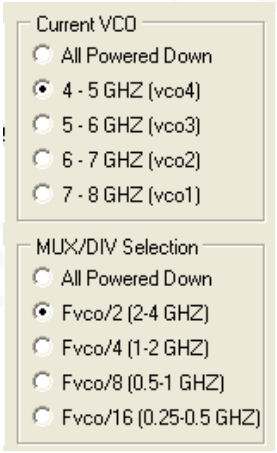

Figure 37 Current VCO and MUX/DIV selections

VCO Capacitance

Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide**.** Selections made when using the **'Calculate'** button however are decided based on the calibration table used in this block.

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

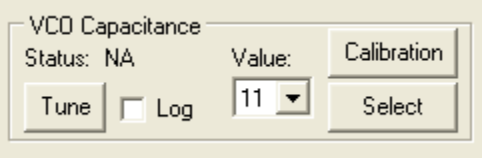

Figure 38 VCO Capacitance

Use of the **'Calibration'** button is described at the end of this section.

Charge Pump(CP) Current and Offset

CP Current and Offset is set based on the selected loop filter and loop BW. For the recommended loop filter (implemented on the evaluation board). Current should be 1200uA and Up Offset 30uA, as shown.

Figure 39 CP Current and Offset

PLL Calibration Data and File

Press the **'Calibration'** button to enter the Frequency vs Capacitance calibration table data.

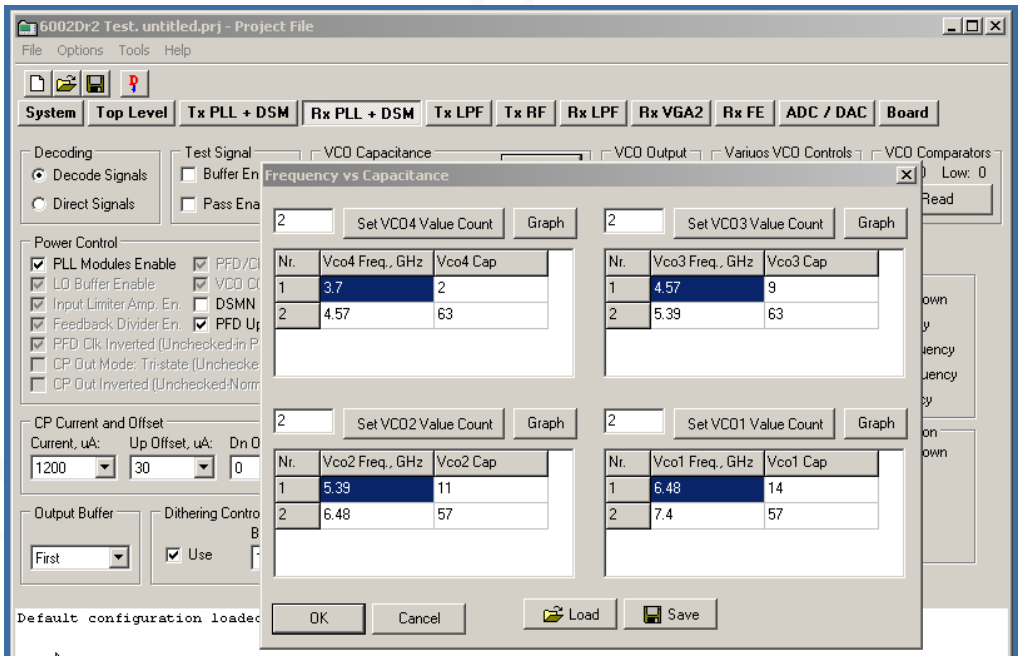

Figure 40 Frequency vs capacitance calibration table data

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The calibration data consists of frequency versus capacitance value responses which are defined by minimum 2 point definition. The loaded VCO file should contain the above data. If not file 'Dr2.vco', provided with SW, should be loaded. To load a new VCO file press the 'Load' button and follow the normal windows procedure to load a file. Then press OK. This new file will now be downloaded on subsequent starts of the software.

4.5.5. Tx LPF

The Tx LPF page contains the SPI controls for the transmitter low pass filters, notably the LPF BW and also the controls for the DC calibration.

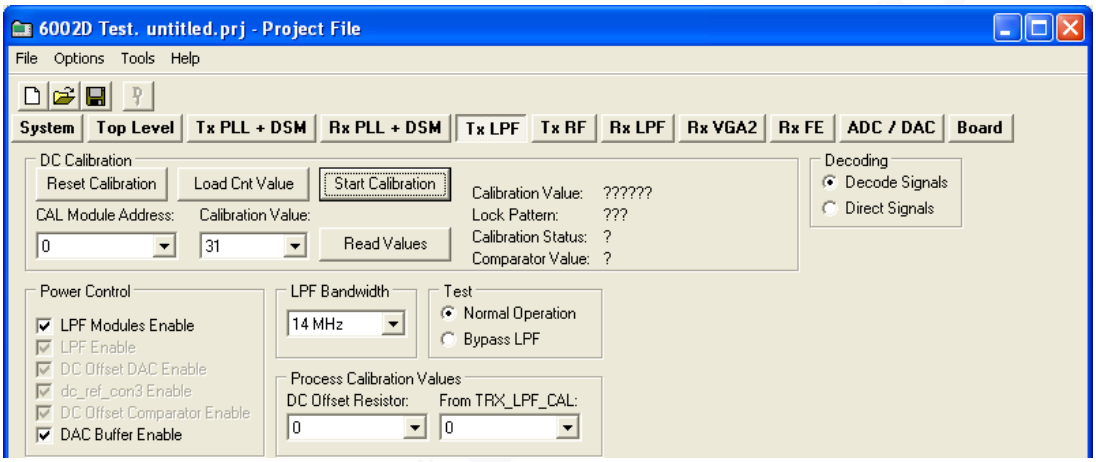

Figure 41 Tx LPF page

Description of each function available from this page is as follows:

DC Calibration

These are the individual controls for the DC correction and auto-calibration routines for the TX LPF (controlled by the 'Transmitter' auto-calibration button on the 'System' page).

The Tx LPF DC calibration has 2 stages which can be calibrated:

- TXLPF(I) at Cal module address 0
- TXLPF(Q) at Cal module address 1

Power Control

Powers down the LPF modules, grayed out controls can be accessed by using direct signals mode.

LPF Bandwidth
Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

Test
Enables LPF bypass for test purposes. Ensure 'Normal Operation' is enabled.

Process Calibration Values
RC calibration values used to process trim the LPF BW. Values are calculated in top level calibration and written into these locations (carried out automatically by 'LPF Core' on 'System' page).

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones are grayed out). 'Decode' mode is recommended.

4.5.6. Tx RF

The TX RF page contains the SPI controls for the TX RF stages, including all Tx gain control, LO correction and Tx output selection.

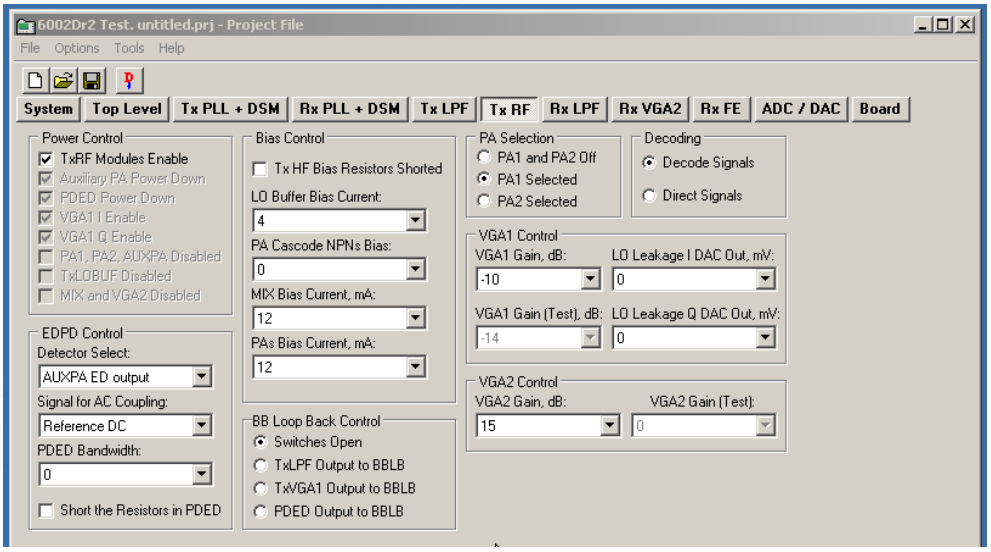

Figure 42 Tx RF page

Description of each function available from this page is as follows:

Power Control
Powers down stages within the Tx RF block – grayed out controls are accessible via 'Direct' decoding mode.

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out). 'Decode' mode is recommended.

VGA1 Control
VGA1 Gain sets VGA1 gain (IF gain stage) from -4 to -36dB via drop down box. VGA1 Gain (Test) sets VGA1 gain in 'Direct Signals' mode by setting 8 bit not log-linear control word directly. 'LO Leakage I DAC Out' and 'LO Leakage Q DAC Out' set DC level injected via the LO correction DACs for LO cancellation.

VGA2 Control
VGA2 Gain sets VGA2 gain (RF gain stage) from 0 to 25dB via drop down box. VGA2 Gain (Test) set VGA2 gain in 'Direct Signals' mode by setting 9 bit not log-linear control word directly.

PA Selection
Select Tx output stage PA1, PA2 or both off.

4.5.7. Rx LPF

The Rx LPF page contains the SPI controls for the receiver low pass filters, notably the LPF BW and also the controls for the DC calibration.

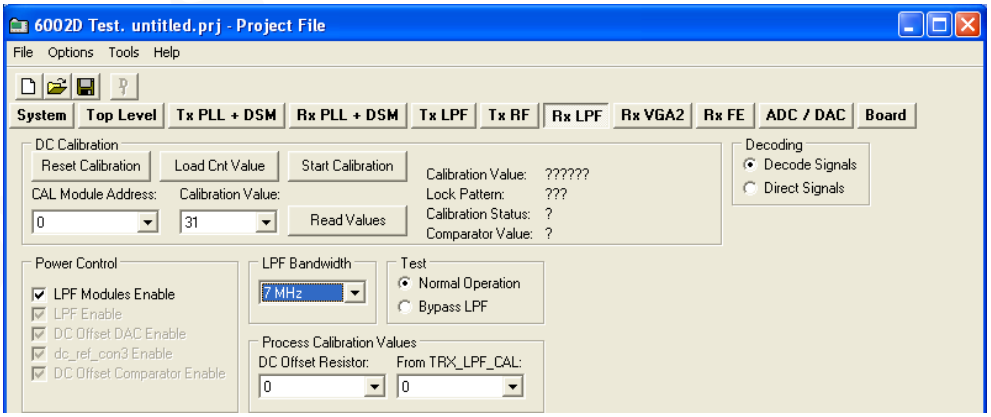

Figure 43 Rx LPF page

Description of each function available from this page is as follows:

DC Calibration

These are the individual controls for the DC correction and auto-calibration routines for the RX LPF (controlled by the 'Receiver' auto-calibration button on the 'System' page).
The Rx LPF DC calibration has 2 stages which can be calibrated:

- RXLPF(I) at Cal module address 0
- RXLPF(Q) at Cal module address 1

Power Control

Powers down the LPF modules, grayed out controls can be accessed by using direct signals mode. Using 'Decode' mode is recommended.

LPF Bandwidth

Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note that RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

Test

LPF bypass for test purposes. Ensure 'Normal Operation' is enabled.

Process Calibration Values

RC calibration values used to process trim the LPF BW, values are calculated in top level calibration and written into these locations (carried out automatically by 'LPF Cal' on 'System' page).

Decoding

Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out).

4.5.8. RX VGA2

SPI controls for the RX VGA2 stage settings.

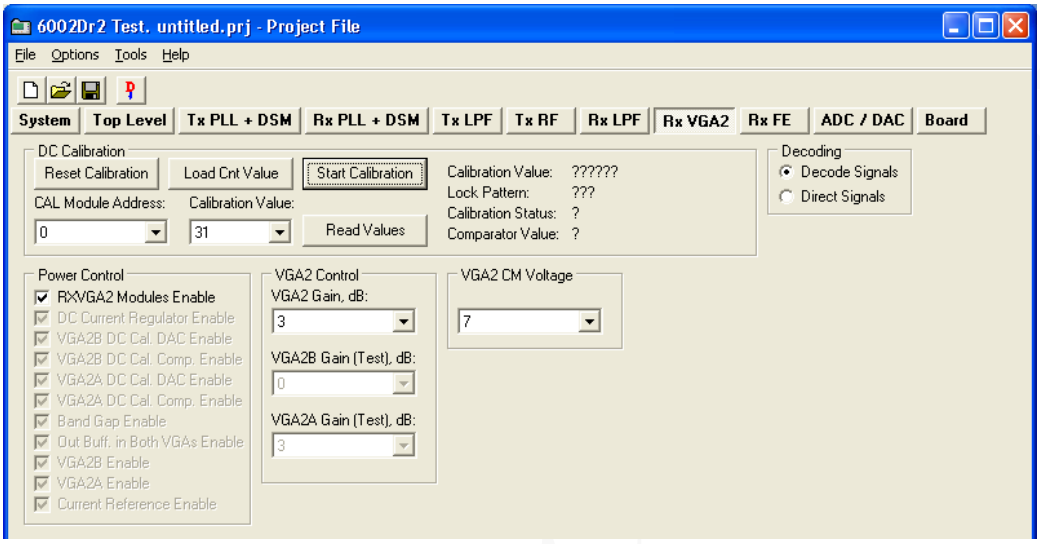

Figure 44 Rx VGA2 page

Description of each function available from this page is as follows:

DC Calibration

These are the individual controls for the DC correction and auto-calibration routines for the RX VGA2 (controlled by the 'Receiver' auto-calibration button on the 'System' page).

The Rx VGA2 DC calibration has 5 stages which can be calibrated:

- RXVGA2 Top at Cal module address 0
- RXVGA2a(I) at Cal module address 1
- RXVGA2a(Q) at Cal module address 2
- RXVGA2b(I) at Cal module address 3
- RXVGA2b(Q) at Cal module address 4

.

Decoding

Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

Power Control
Powers down the RXVGA2 modules, grayed out controls can be accessed by using direct signals mode.

VGA2 Control
Sets RXVGA2 Gain, available range is 0 to 30dB in 3dB steps. Decoding is set to 'Decode Signals' for normal use.

VGA2B Gain (Test) and VGA2A Gain (Test) are available in test mode to control A and B stages directly. Decoding is set to 'Direct Signals' to use this function. This feature is not used for normal operation.

VGA2 CM Voltage
Sets RXVGA2 output common node voltage to interface to ADCs. Code 12, which corresponds to 780mV, is recommended.

4.5.9. RX FE

Sets the SPI controls for the RX Front End stages, including LNA selection, LNA gain, RXVGA1 gain and RX LO cancellation.

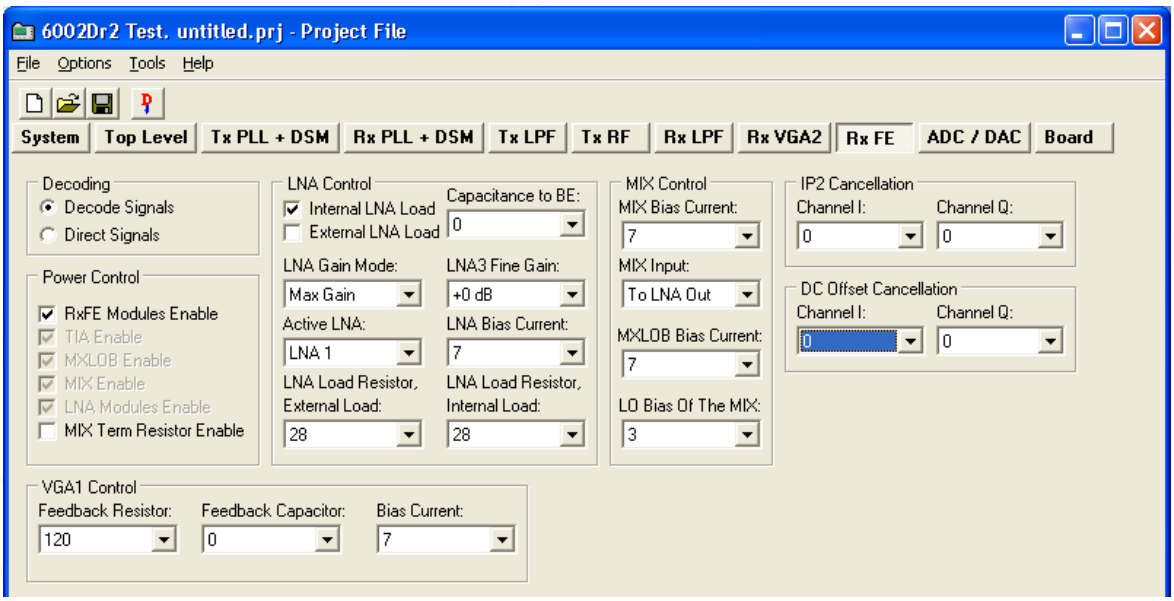

Figure 45 Rx FE (Front End)

Description of each function available from this page is as follows:

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out).

Power Control
Powers down the RXFE modules, grayed out controls can be accessed by using direct signals mode.

DC Offset Cancellation
Applies DC level to mixer output to cancel DC level from LO leakage.

IP2 Cancellation
Applies offset to mixer to improve IP2 performance. Not required.

LNA Control
Settings for LNA controls are as follows:

- Internal/External LNA load tick boxes – use internal.
- Capacitance to BE – leave as default (0)
- LNA Gain Mode – selects LNA gain, Max, Mid and Bypass.
- LNA3 Fine Gain – fine gain setting for LNA3 which has no bypass mode, 0 to + 3dB.
- Active LNA – Select active LNA 1 to 3, also need to change the RX LO buffer in 'RX PLL + DSM' page when changing LNA. This control changes RX LO buffer automatically.
- LNA bias current – leave at default (7).
- External load – not used when Internal load selected.
- Internal Load (0 to 63) sets LNA gain, max (0dB) = 55, min (-9.2dB) = 0. Do not set above 55.

See figure below for settings

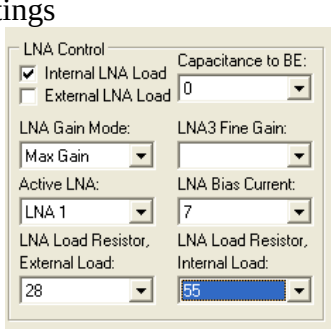

Figure 46 LNA Control setting

MIX Control

Settings for Mix control are shown below, do not change:

- MIX Bias current – '7', leave it at default.
- MIX Input – 'To LNA Out', leave it at default.
- MXLOB Bias Current – '7', leave it at default.
- LO Bias Of The MIX – '3', leave it at default.

See figure below for settings

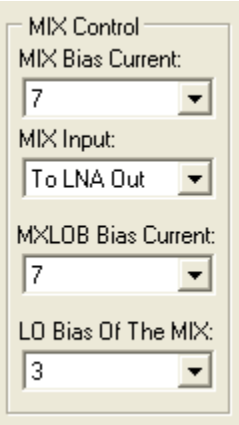

Figure 47 MIX Control settings

VGA1 Control

Feedback Resistor (0 to 123). Only use settings up to 120
Sets VGA1 gain, max (0dB) = 120, min (-24dB) = 0, so do not set above 120. Gain control is not log-linear.

Feedback capacitor (0 to 123)
Introduces a single pole LPF at VGA1 output. Bandwidth dependent on 'Feedback resistor' and 'Feedback capacitor'. For no filtering leave at default (0).

Bias Current - leave at default (7).

4.5.10. ADC/DAC

ADC / DAC page sets all the controls for the data ADCs in the receive path and data DACs in the transmit path.

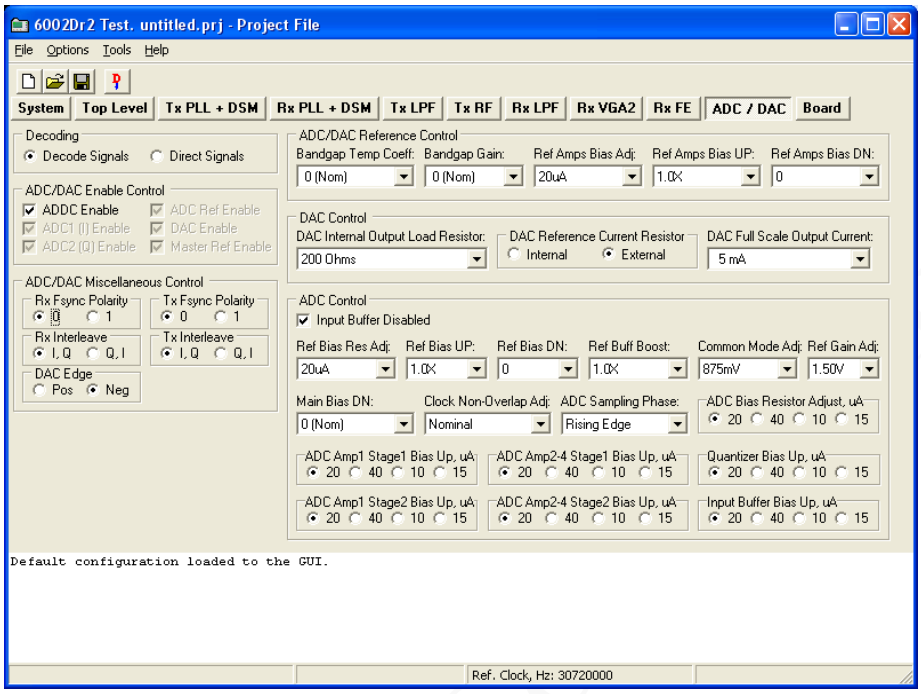

Figure 48 ADC/DAC page

Description of each function available from this page is as follows:

Decoding

Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options, the available options are highlighted (and the unavailable ones are grayed out).

ADC/DAC Miscellaneous Control

Rx Fsync Polarity – sets the polarity of the RX IQ SEL signal for the first sample of the Rx IQ pair.
Rx Interleave – sets the order of the RX IQ pair.
Tx Fsync Polarity – sets the polarity of the TX IQ SEL signal for the first sample of the Tx IQ pair.
Tx Interleave – sets the order of the TX IQ pair.

See diagram below for explanation:

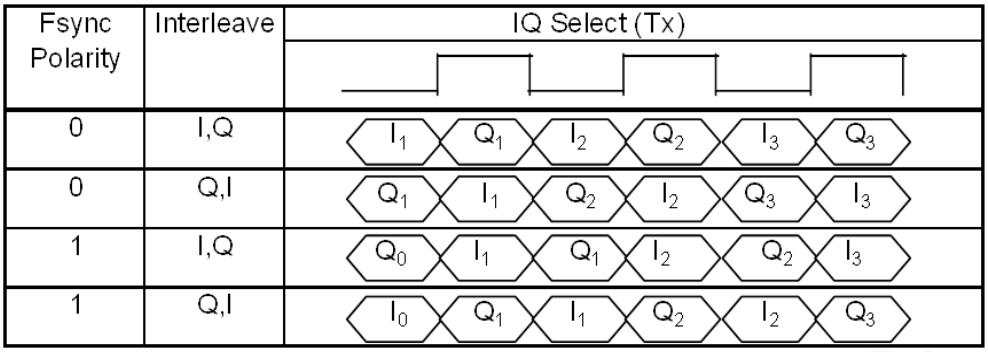

Figure 49 DAC enable control timing for TX

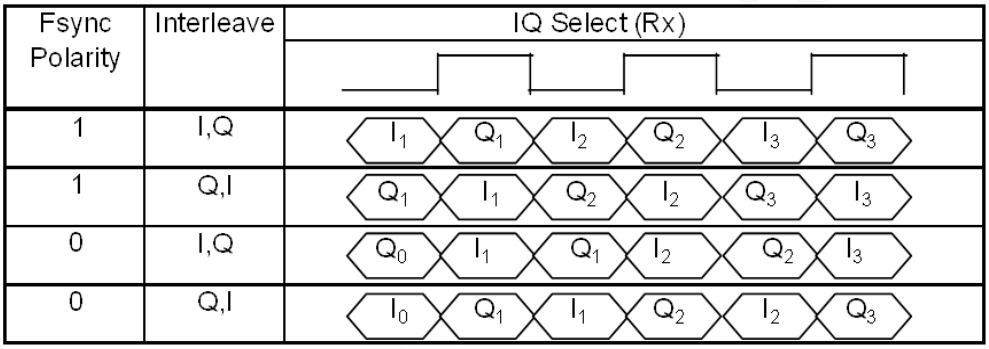

Figure 50 ADC enable control timing for RX

DAC Edge

DAC Edge – selects the edge of the DAC clock which the data is clocked from. Negative is usually required.

ADC/DAC Enable Control

Check 'ADC Enable' to enable ADCs and DACs. Sub-blocks are also independently controllable in 'Direct Signals' mode.

DAC Control

- Internal output Load Resistor 50, 66, 100, 200 Ohms or Open Circuit setting (when using external load resistor).
- DAC Reference Current resistor – use External.
- DAC Full Scale Output Current (2.5, 5, 10mA). Use Load resistor and Full scale output current to control DAC output voltage swing.

ADC/DAC Reference Control

Use default settings:

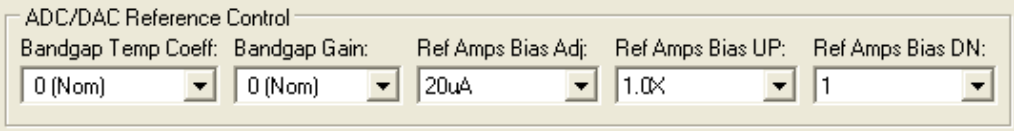

Figure 51 ADC/DAC Reference control – default settings

ADC Control

Use default settings with following exceptions:
Ref Bias Res Adj = 10uA (minimizes ADC noise)
Common mode Adj = 960mV.
Ref Gain Adj = 1.75V.

See diagram below for settings including the exceptions listed above which have been highlighted in red.

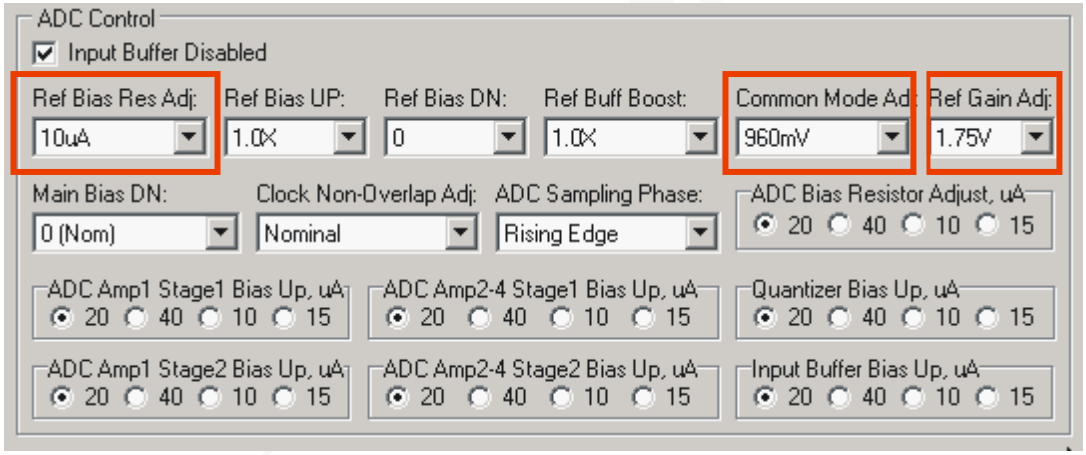

Figure 52 ADC Control settings

4.5.11. Board

Board refers to the interface board. This page provides the SPI control via a second enable pin on the SPI interface for an external PLL chip. The purpose of this is so the interface TCXO can be locked to external test equipment if required.

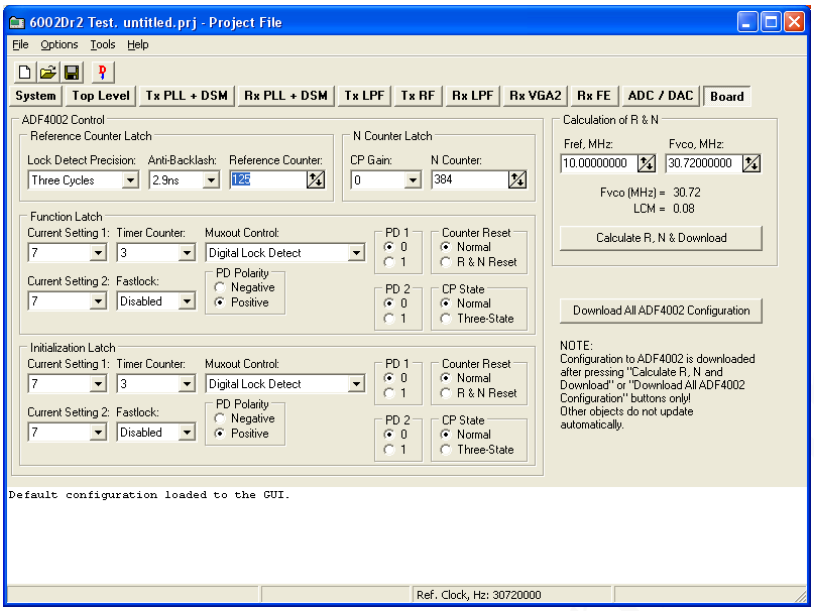

Figure 53 S/W control for on board ADF4002 – TCXO locking

The default settings will program the standard board with a 30.72MHz TCXO and a 10MHz reference.

Using this feature:

- Press ‘Download All ADF4002 Configuration button’

Then:

- Press ‘Calculate R,N & Download’ button to program the ADF4002, if all is correct the green PLL locked LED (LD1) on the interface board should illuminate. LD1 is located in the upper left hand corner of the interface board.

5

Transmitter and Receiver Basic Setup

5.1 Transmitter Setup and Basic Testing

This is a quick check without the need to connect to an external baseband interface. The test using DC to provide LO leakage to test the Tx chain, for accurate repeatable measurements the Baseband Interface (data DACs) should be set to a known state. Also, verify the reference clock frequency is set properly. The reference clock frequency can be set in the top "Options" menu under "Reference Clock". It is typically set to 30.72 MHz but can vary depending upon the frequency of the TCXO installed on the evaluation board.

5.1.1. Top Level Setting

Using the "Top Level" page. Verify the "Tx DSM SPI" Clock Buffers and the "Soft Tx Enable" Power Control are enabled in the menus as shown below.

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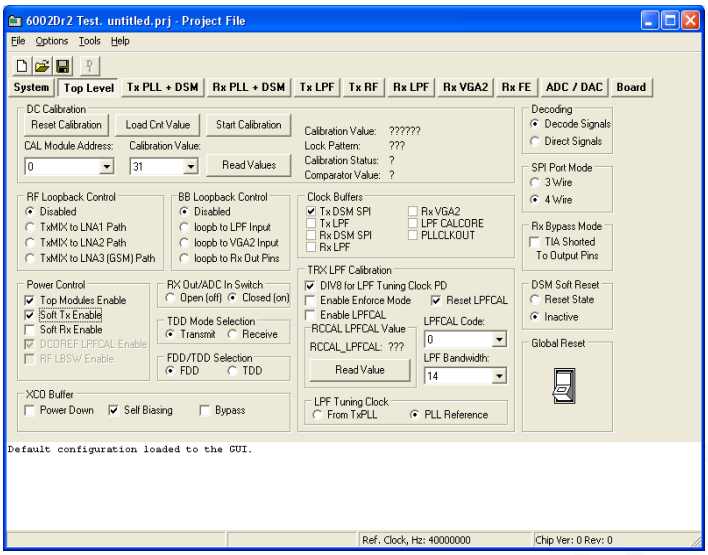

Figure 54 Top Level Settings

Note: The LMS6002 communication can be easily checked by toggling the "Soft Tx Enable" in the Power Control section. The current change can be observed on power supply display.

5.1.2. TX LPF & Gain Setting

Using the 'Tx LPF' page. Set the LPF bandwidth to your desired value; see figure below, example setting is 14 MHz.

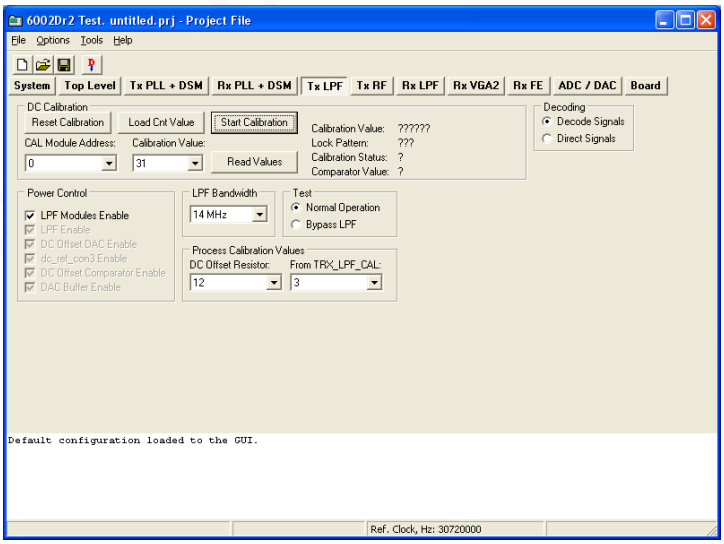

Figure 55 Setting Tx LPF bandwidth

Select Tx RF page to set gain and select Tx Output. For basic operation select the following

- VGA1 gain = -10
- VGA2 gain = 15
- PA1 Selected

See diagram below to check selections.

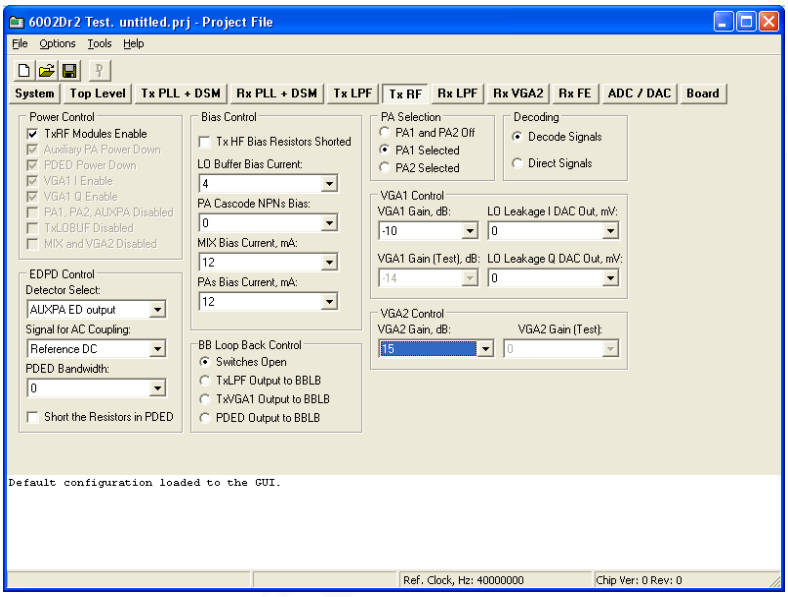

Figure 56 Tx gain setting and PA selection

5.1.3. TX PLL Setup

Select Tx PLL + DSM page to set up the Tx PLL. Please follow the instructions 1 to 3 below in the order shown and illustrated in the figure below.

1. Set **'Output frequency'** (Tx frequency), example shown = 2.14GHz and then press **'Calculate'**, note divider ratios should change.
2. Change **'CP Current and Offset'** (CP = Charge Pump) to the following:
   a. Current , uA = 1200uA
   b. Up offset, uA = 30uA
3. Press "**Tune**" to fine tune VCO capacitor selection. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

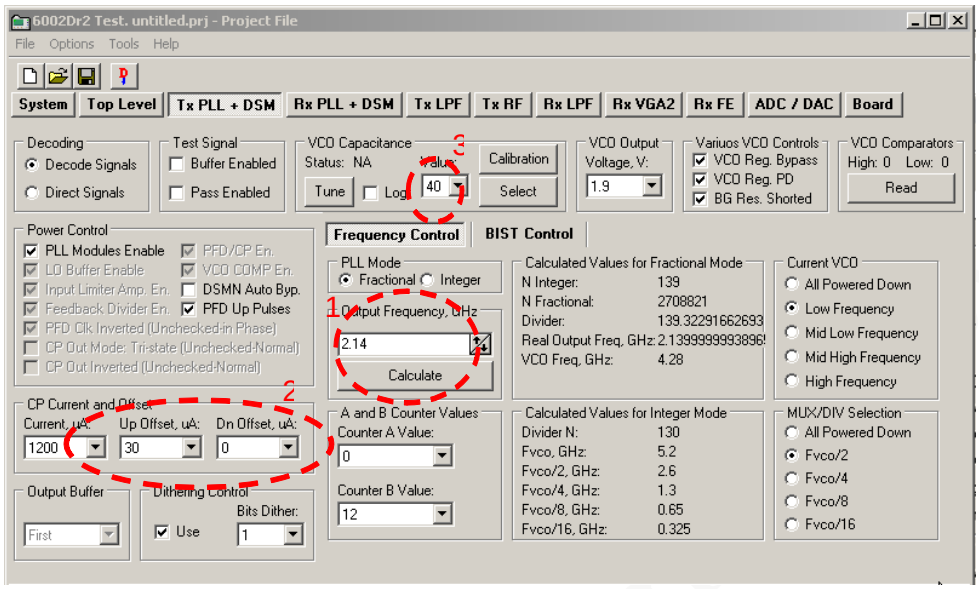

Figure 57 Tx PLL setting

5.2 Testing TX Output

When transmitter is configures as it showed in section 5.1, one of your selected TX output can be connected to spectrum analyzer (SA). In SA you can now observe the results of this basic operational test. The test is looking at the DC offset from the un-programmed data DAC as LO leakage and the example shown below is measuring a value of 2.1dBm. As the DACs are not programmed yet levels may be different from the screen shot example.

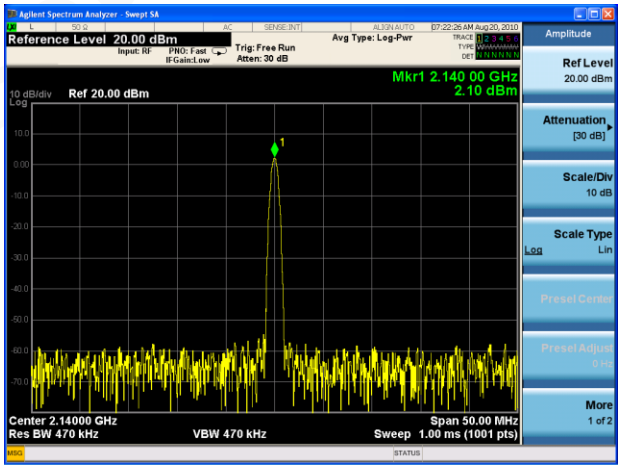

Figure 58 Basic TX testing using DC offset resulting in LO leakage

5.2.1. TX Basic Operation Checks

To check basic TX frequency and gain control conduct some tests changing frequencies and gain settings. The following four tests are recommended:

TX RF – VGA 1 change setting from -4 to -35 and observe results. LO should vary by approx 1 dB steps, 31dB range.
TX RF – VGA 2 change setting from 0 to 25 and observe results. LO should vary by approx 1 dB steps, 25 dB range.
Change frequency from 2.14GHz to 2.11 GHz and press '**Calculate'/'Tune'** (CAP value should change), check Spectrum Analyzer.
Change frequency from 2.11GHz to 2.17 GHz and press '**Calculate'/'Tune'** (CAP value should change), check Spectrum Analyzer.

5.3 Receiver Setup and Basic Testing

Basic functionality checks on the receiver side are achieved by using the analogue output from connector J3, not using the digital output from the data ADCs.

5.3.1. Top Level Settings

Using the "Top Level" page, verify the "Rx DSM SPI" Clock Buffers and the "Soft Rx Enable" Power Control is enabled in the menus as shown below. Also verify the RxOut/ADC in Switch is set to Closed.

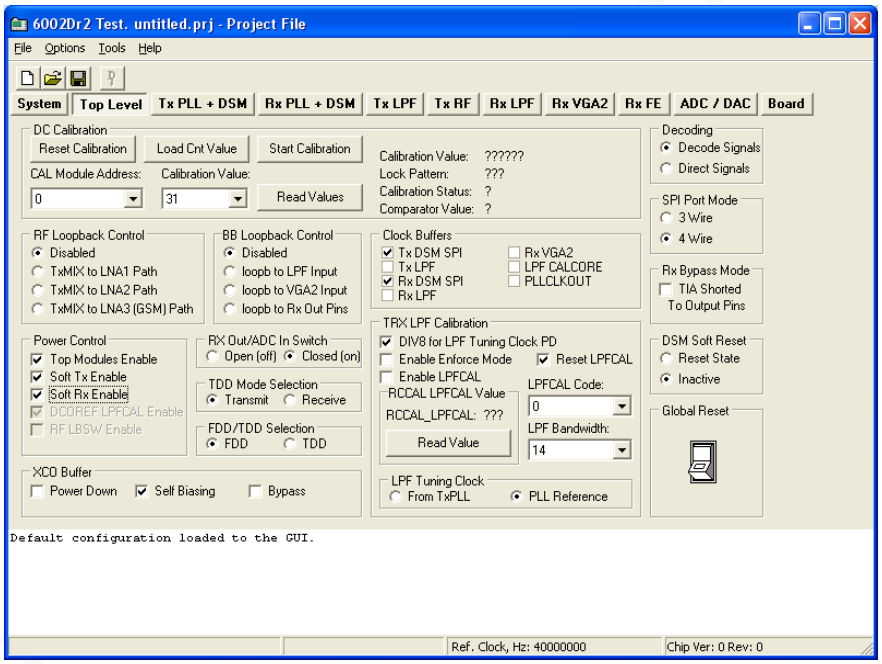

Figure 59 Top Level Settings

5.3.2. RX LPF & Gain Setting

Set LPF bandwidth to 7MHz as illustrated in figure below.

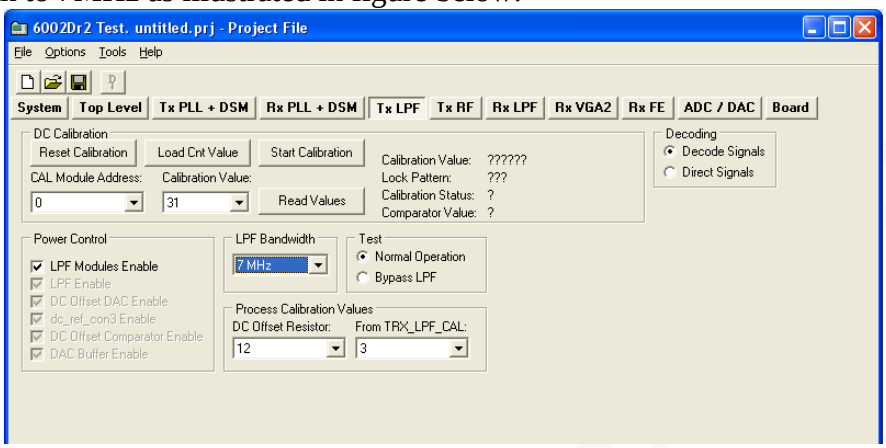

Figure 60 Setting Rx LPF to 7 MHz

Select '**Rx VGA2 page'** to set the gain. For basic operation set VGA2 gain = 30. See figure below.

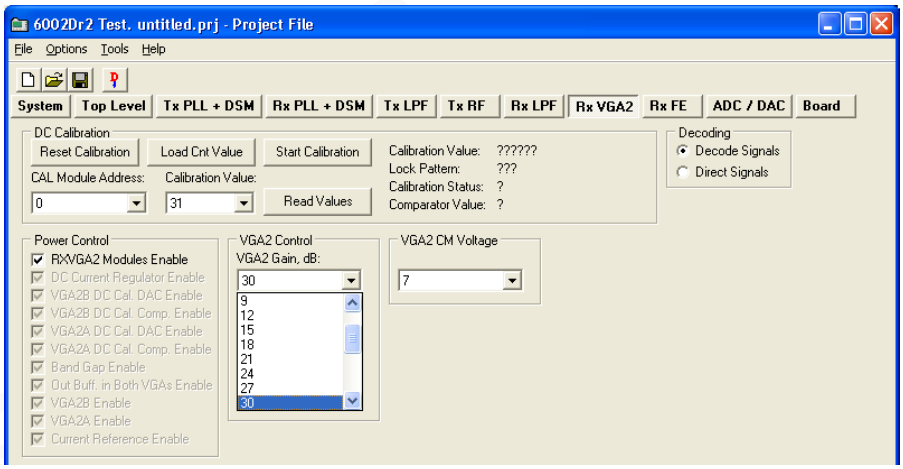

Figure 61 Setting Rx VGA2 gain

Select '**RX FE page'**, check **'VGA1 Control Feedback Resistor'** is set to 120 (Default setting). The feedback resistor controls the gain of VGA1. Set LNA gain by using **'LNA load resistor – Internal load',** set to 55.
Check **'Active LNA'** = LNA1 and **'LNA Gain Mode'** is set to Max Gain.

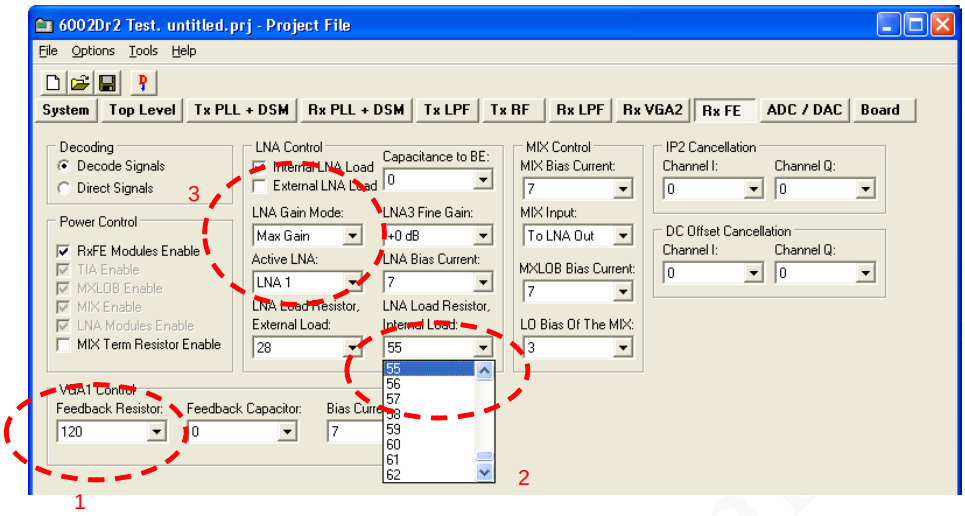

Figure 62 Rx LNA and VGA1 settings

5.3.3. RX PLL Setup

Select **'Rx PLL + DSM'** page to set up the Rx PLL. Please follow the instructions below in the order shown and illustrated in the figure below.

a. Set **'Output Frequency'** (Tx frequency), example shown = 1.95GHz and then press **'Calculate'**, note divider ratios should change.
b. Change **'CP Current and Offset'** (CP = Charge Pump) to the following:
a. Current , uA = 1200uA
b. Up offset, uA = 30uA
c. Press "**Tune**" to fine tune VCO capacitance. If you want to observe the VCO capacitor selection algorithm results select "**Log**".
d. Make sure that '**Output Buffer**' is set to First.

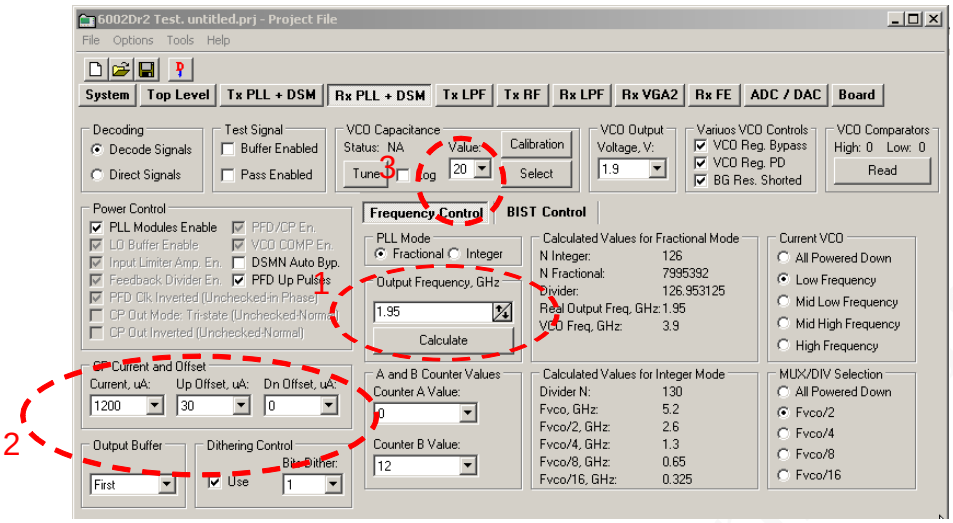

Figure 63 Rx PLL settings

5.4 Testing RX Output

Set the signal generator to 1951MHz (1MHz offset from PLL frequency selected) and input a sine wave at -60dBm into the reference board antenna connector (connector J2).
Configure receiver as showed in section 5.3. Connect an oscilloscope to J3.20 or J3.18 on the evaluation board. Correct operation will results in two sine waves, 90° out of phase, being displayed. If the sine wave output for I and Q can be seen then the receiver is operational. See figure below.

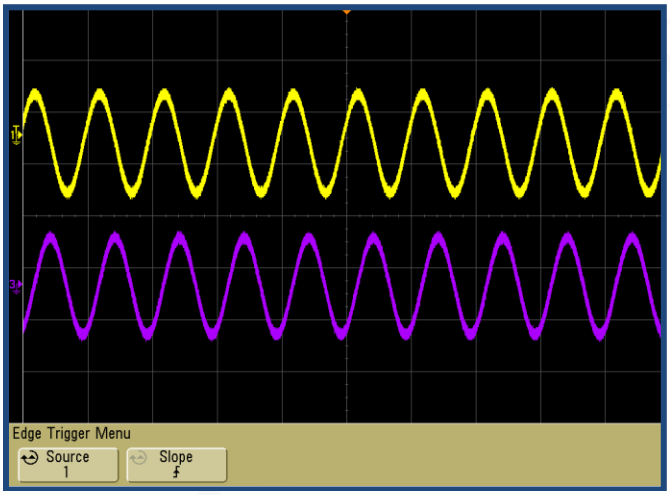

Figure 64 Oscilloscope capture of 1 MHz I & Q Sine wave outputs

5.4.1. RX Basic Operation Checks

To check basic Rx frequency and gain control conduct some tests changing frequencies and gain settings. The following six tests are recommended:

a. RX VGA2 – VGA 2 change setting from 30 to 0, observe results, gain should decrease.
b. RX FE – VGA 1 change feedback resistor from 120 to 0, observe results, gain should decrease.
c. RX FE – LNA gain change from Max to Mid, observe results, gain should decrease.
d. RX FE – LNA gain change from Mid to Bypass, observe results, gain should decrease.
e. Change frequency from 1.95GHz to 1.92GHz and press '**Calculate'/'Tune'**. Change Signal Generator to 1.921GHz (1MHz offset from PLL). Observe results.
f. Change frequency from 1.92GHz to 1.98GHz and press '**Calculate'/'Tune'**. Change Signal Generator to 1.981GHz (1MHz offset from PLL). Observe results.

6

LMS6002D Calibration Procedures

6.1 TX LO Leakage Calibration

This procedure assumes the transmitter has been turned on and initialised, it describes how to then use the parameters within the LMS6002D to cancel any LO leakage from the IQ modulator.

It is intended that this will be a single point calibration per band, the example given uses 3GPP Band I with a centre frequency of 2140 MHz.

The transmitter should be set up with the following parameters:

Parameter	Page	Value
Transmitter Frequency	System Interface	2140
Soft Tx enable	Top Level	tick box selected
Tx DSM SPI clock buffer	Top Level	Tick box selected
LPF bandwidth	Tx LPF	3.5MHz
PA1 selected	Tx RF	PA1 Selected
VGA1 gain	Tx RF	-10
VGA2 gain	Tx RF	15

Table 8 Transmitter setup

No signal should be applied to DAC's or DC Low signal, generated by BB can be applied. The previous method is more preferable. Note: Set gain settings before calibration.

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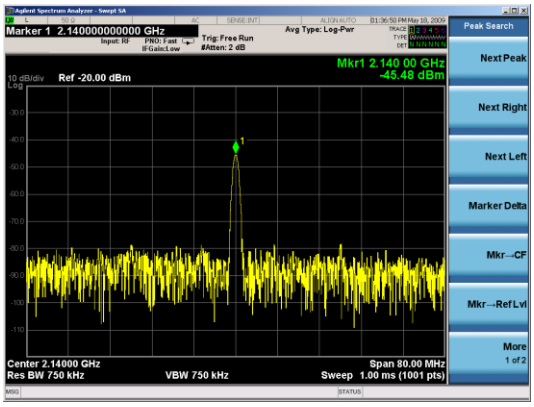
The output should be observed on the spectrum analyser.



The signal on the screen represents the LO feedthru from the transmit modulator.

In this case the level is -45dBm

Figure 65 Transmit Output

Assuming the LPF Core calibration has been carried out in the initialisation then press the 'Transmitter' button on the System Interface page in the Automatic Calibration area.

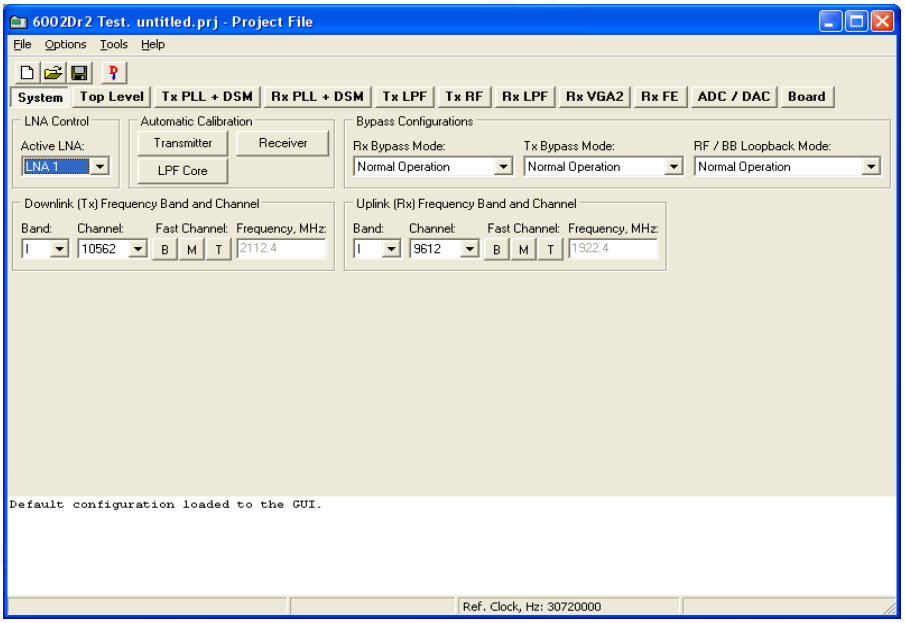


Figure 66 System Window. Use Automated Calibration

'Tx Calibration Done' should appear in the text box in bottom of the display.

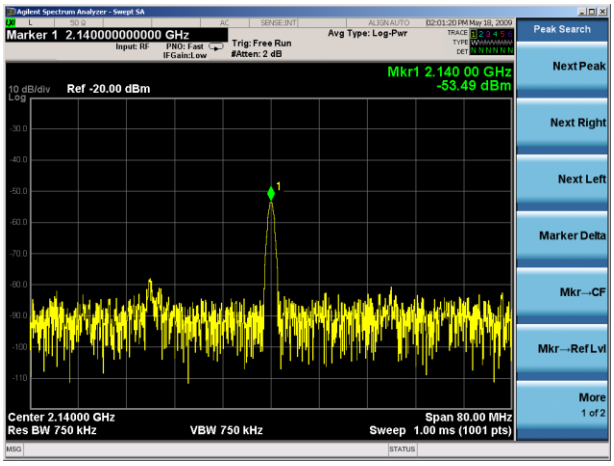


Figure 67 Transmit Output After Calibration

In this case the LO dropped after automatic calibration to -53dBm as shown in Figure 67.

Note. Automatic calibration is intended to make the DC zero at the output of the LPF, this is not the same as cancelling the LO, it just makes the DC contribution from the IQ chain as low as possible.

It may be the case that the level will go up after automatic calibration – do not worry if it does, this is due to the default values on power up cancelling the LO at the selected frequency.

Select the 'Tx RF' page in the SPI software.

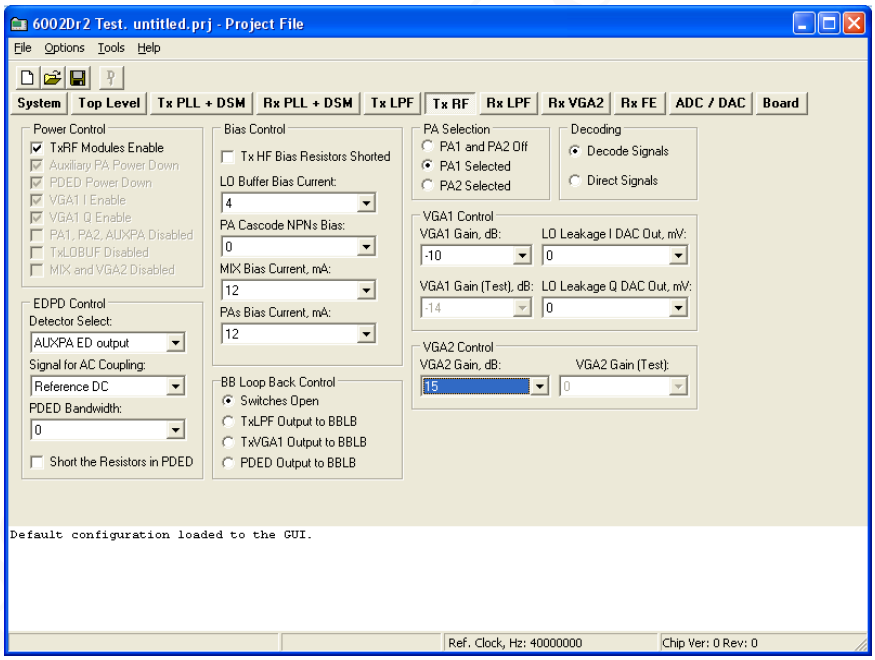


Figure 68 Tx RF window

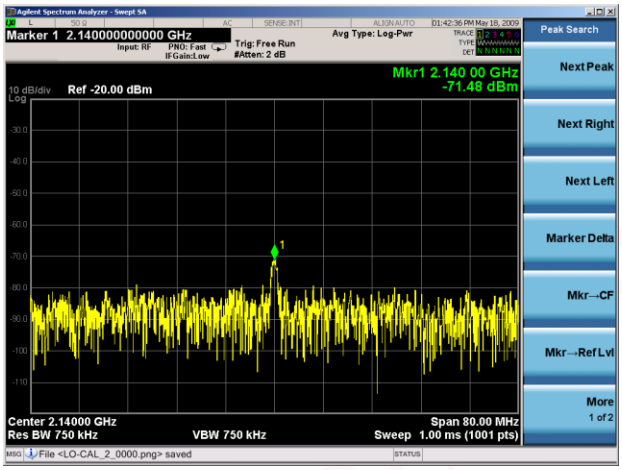
The LO cancellation DACs level is in the boxes marked' 'LO Leakage DAC I Out' and 'LO Leakage DAC Q Out'. The entry mechanism is different to the LPF DC offset and easier to tune.

LO Leakage DAC I/Q Out boxes contain the value of the DC LO cancellation DAC in mV and ranges from -16 to 15.875.

Click on the VGA1 DC shift box, a drop down menu appears, click again and the drop down menu collapses leaving the entry box blue.

The value in the box can now be adjusted using the up and down arrows on the key board, once the number has changed the register in the LMS6002D is updated, allowing for a simpler search method.

a. Select the I DAC box
b. Increase / decrease until minimum is found.
c. Do same for Q.
d. It is possible that 0 is the best result for both as the optimum has been found during the LPF calibration above.



In this case the LO cancellation has been improved to -71dBm as shown in this figure. The optimum values were:

I = 0
Q = -0.125

Figure 69 Transmit output after calibration

6.2 Transmit I/Q Balance Calibration

This procedure assumes the TX LO calibration procedure in section 6.1 has been completed. The purpose of this calibration is to optimize I/Q balance for optimum transmit EVM performance. Typically, this is done by applying a 1 MHz CW tone from a digital I/O card through the digital interface at J5. The 1 MHz CW tone could also be applied at J3 from a differential I/Q analog signal generator.

Initially, the user should observe a spectrum at the tuned frequency that is similar to the figure below.

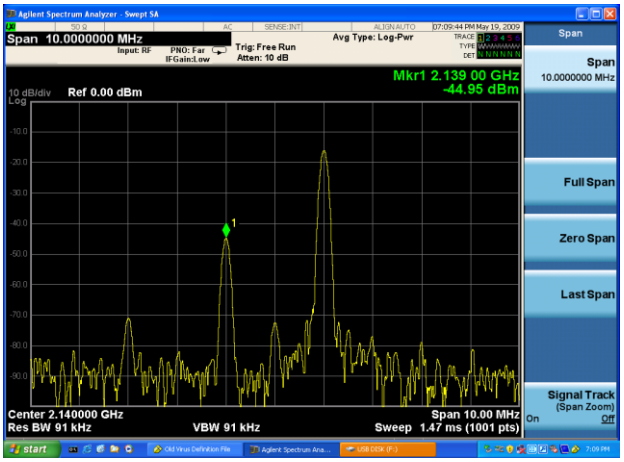


Figure 70 Initial -1 MHz Image Spectrum

The wanted signal can be seen at 1MHz offset from the selected RF frequency (2140MHz), In this case at a level of approx -16dBm.

The unwanted (lower) sideband can be seen at -1MHz offset, with no correction is at a level of -45dBm (29dBc)

Note – the 3rd order product at LO-3*1MHz can be seen also.

The image or sideband rejection performance of the system depends upon the phase and gain match of the I and Q paths. This includes the test equipment, cables and of course the LMS6002D transmit path. The closer in length the cables between the signal generator and the test board are the better.

The phase match also depends on the accuracy of the sin/cosine split on the LO of the IQ modulator (inside the LMS6002D), the bulk of the phase correction is for this parameter – hence, amplitude mismatch will vary little with frequency, however phase mismatch may be quite different for each band.

The result of the phase angle calibration can be seen below.

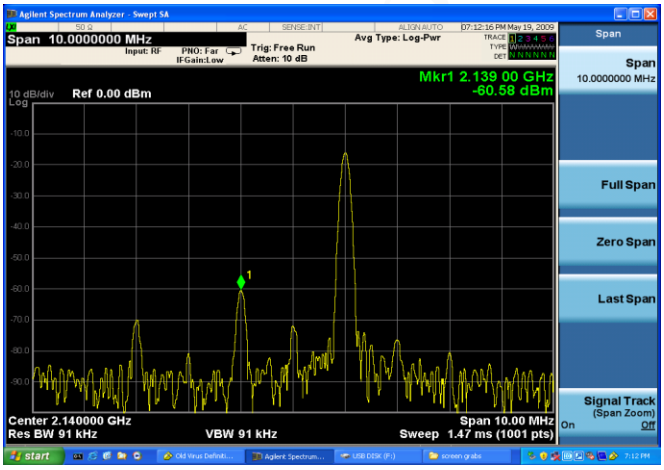


Figure 71 Phase angle calibration

The result of the phase angle calibration is seen.

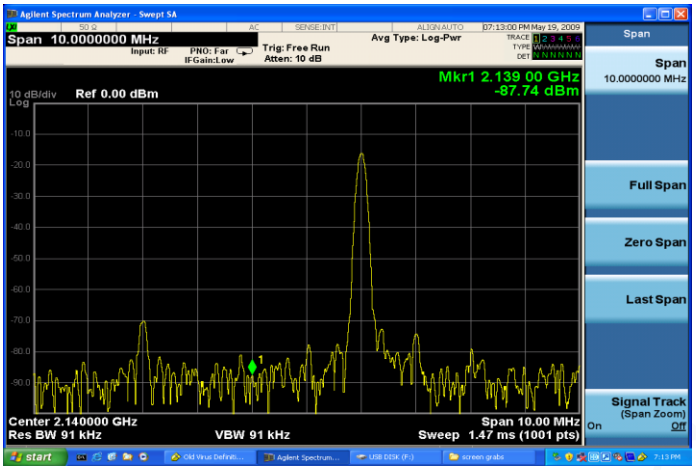
The unwanted sideband has been reduced to -60dBm (-44dBc).

The optimum value found in this case was 4.1 deg.

The result of the amplitude balance calibration is seen.

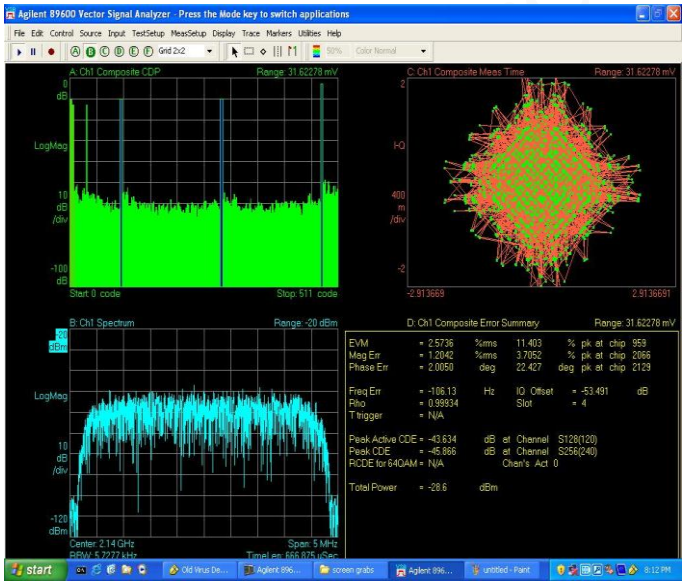
The unwanted sideband has been reduced to <-80dBm (-64dBc).

The optimum value found in this case was 0.11 dB.



If necessary repeat the phase and amplitude adjustments until the optimum values are found and an EVM ≤ 4% is measured as shown below. The transmit I/Q balance calibration is valid on the flat part of the LPF bandwidth. As you approach the LPF corner frequency the lower sideband cancellation will begin to degrade. For example, with the 1 MHz tone used in this calibration the EVM will degrade as the filter bandwidth decreases below 1.92 MHz.

Figure 72 Amplitude balance calibration



Using the VSA analysis software.

WCDMA TM2 codes can be seen in top left.

Spectrum, bottom left

Composite constellation, top right.

Signal statistics, Bottom right.
EVM 2.5%
Peak CDE -45 dB

Figure 73 Transmit EVM performance after calibration

Note: The EVM is dependent on a number of parameters being set up correctly. Phase noise performance of the LO is dominant factor in the above measurement.

6.3 Receiver DC Calibration

The receiver has a number of self-calibration routines which are designed to cancel out DC offsets from the LPF's and the VGA's. In addition it has I and Q LO cancellation DACs which can cancel out the DC caused by the LO leakage in the mixers.

It is similar to calibration in the transmit path where the low LO levels are easy to measure with the spectrum analyser but low DC levels are more difficult to measure.

In most cases the baseband (BB) processor is capable of adjusting the DC calibration (and also the IQ phase and amplitude match) based on measurements of the uplink signal. It is only necessary to ensure the calibration is good enough so the ADC is not at full scale.

However for testing without the BB the following procedure has been devised. This method uses the I and Q samples from the oscilloscope. The Agilent VSA software is used to sample the oscilloscope and display the spectrum. The oscilloscope used for this procedure must be supported by the Agilent VSA software. The spectrum analyser cannot be used because it cannot display DC.

1. Set the receiver up as in section 5.3.
2. Resetting DC Calibration.
   In 'Rx FE' Tab, set RXVGA1 I and Q DC Offsets to middle value 0.

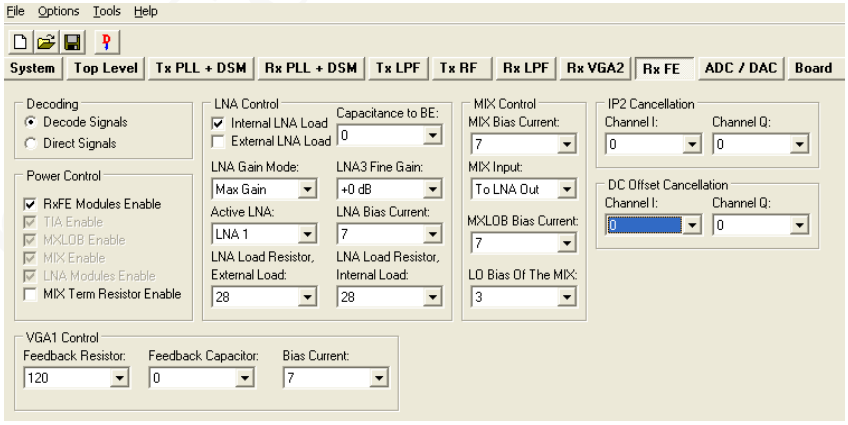


Figure 74 Rx FE page

3. In ‘Rx LPF’ Tab, press “Reset Calibration”.

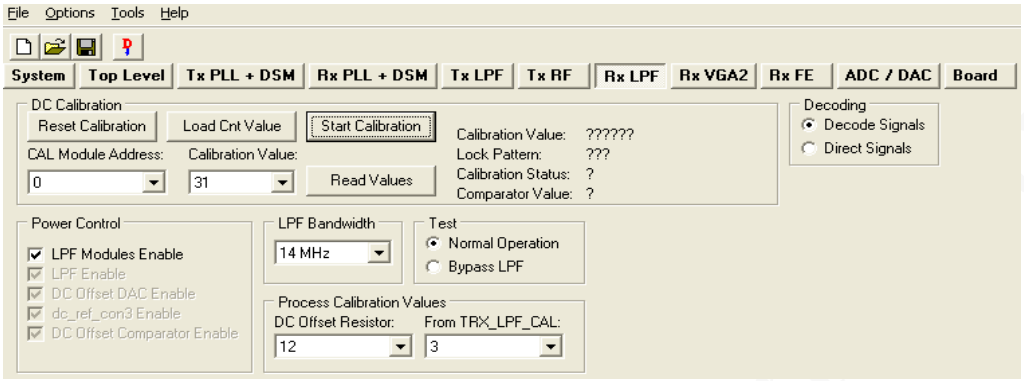


Figure 75 Rx LPF tab

4. In ‘Rx VGA2’ Tab, Press “Reset Calibration”.

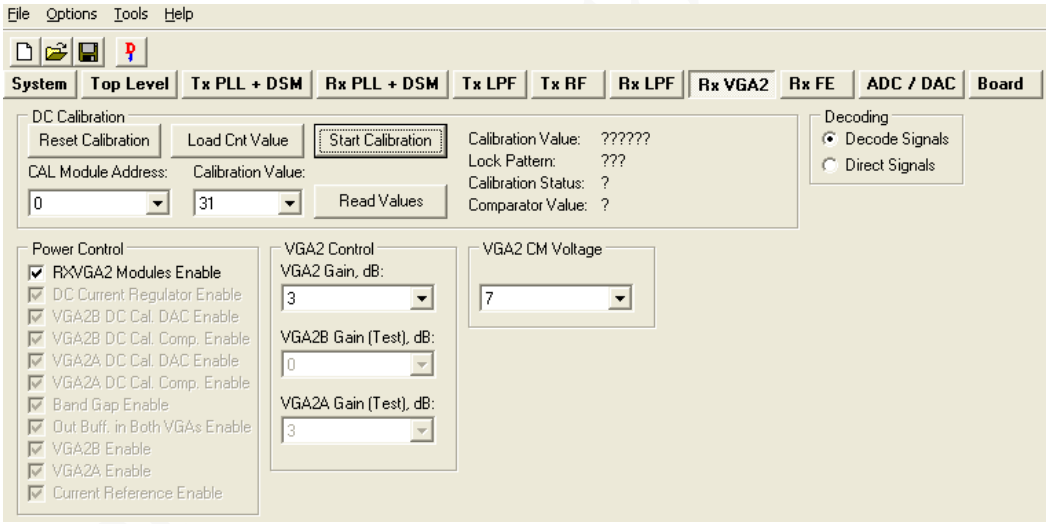


Figure 76 Rx VGA2 Tab

DC Leakage after Calibration Reset.
DC offset very large – would prevent automatic DC calibration.

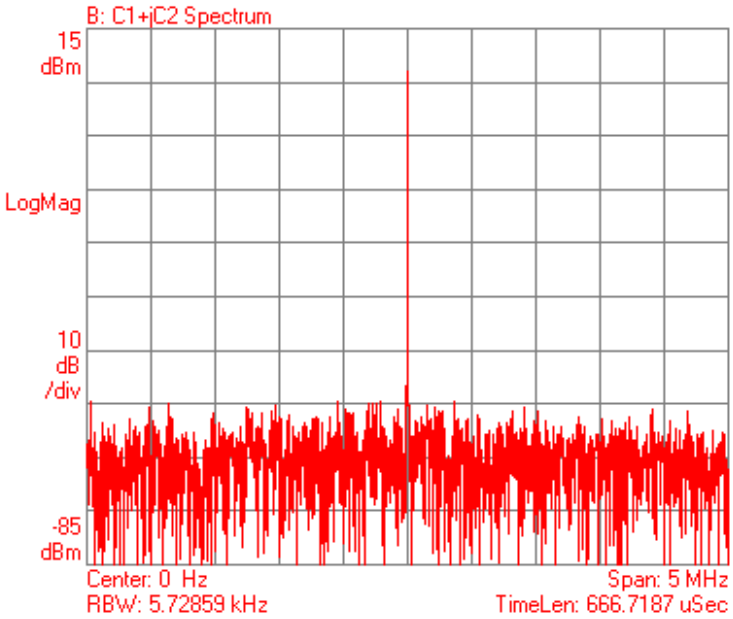


Figure 77 Receiver LO leakage

5. RXVGA1 Offset Optimisation
   In 'RX FE' tab, slightly adjust the RXVGA1 DC offset values to reduce the DC offset.

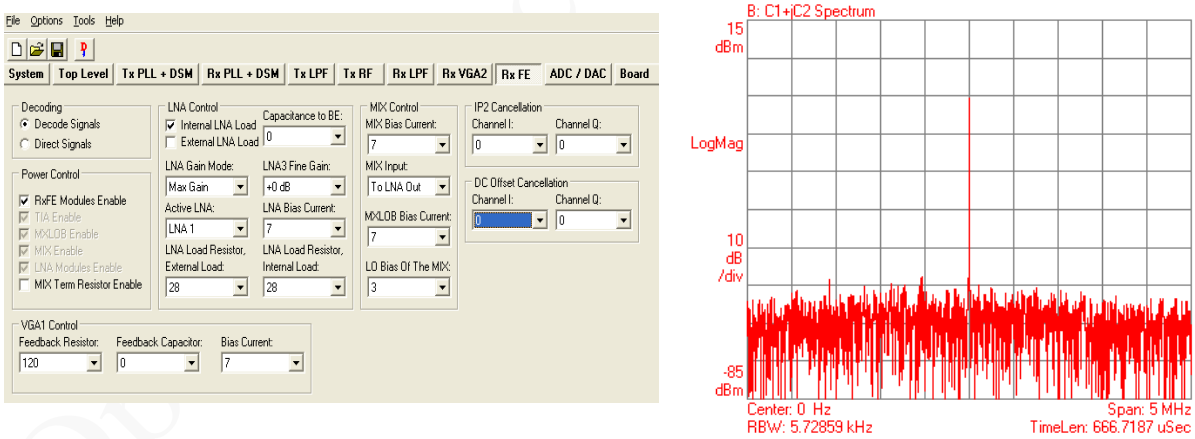


Figure 78 Rx VGA1 DC Offset Adjust in RX FE Tab

6. Automatic DC Calibration

   If RX VGA1 DC Offset is small enough, automatic DC calibration can be used in System Interface, select receiver automatic calibration.

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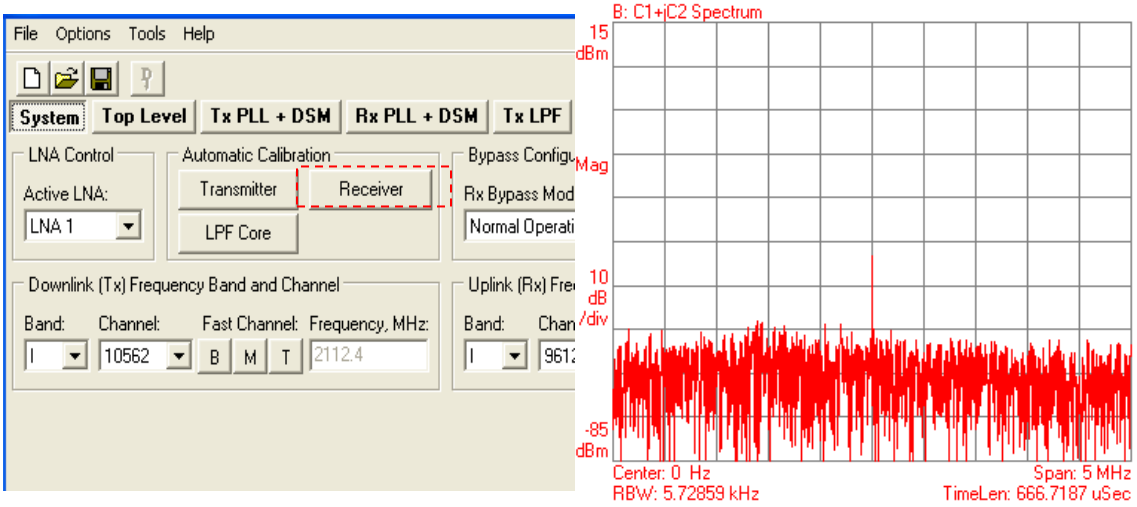

Figure 79 Rx automatic DC calibration result

6.4 Calibration Process Summary

There are several similarities between receive and transmit DC calibration process but one fundamental difference. During the transmit calibration process no signal can be applied to the input of the transmitter. An automated DC calibration is performed to ensure the BB stages contribute no DC offset to the LO leakage calibration. Finally, an LO leakage calibration is performed to minimise LO leakage. The transmit input must be zero so that the automated DC calibration can find the correct minimum DC point. This DC calibration process provides optimum transmitter performance.

In the receiver a similar DC calibration process is applied but in reverse order. When no signal is applied at the input of the receiver, the resulting DC offsets at the receiver outputs are due to LO leakage (multiplied by the RX gain) and the DC offsets in the LPFs and VGAs. The first step is to calibrate the LO leakage contribution and minimise the DC offset due to LO leakage. After the DC offset due to LO leakage has been removed then the automated DC offset calibration routines can be run. These DC offset calibration routines will remove the DC offset contribution from the LPFs and VGAs. This calibration process will result in minimum DC offset in the receiver and optimum sensitivity and dynamic range.

7

Appendix A – Saving and Retrieving SPI Test Setups

The LMS6002D chip set up can be stored in a *.prj file and used in the future. The Save Project feature of the software tool allows all the SPI settings to be saved for future use.

7.1 Saving a Setup

To save the SPI setup being used, press the File button on the toolbar. Select “Save Project” as shown below.

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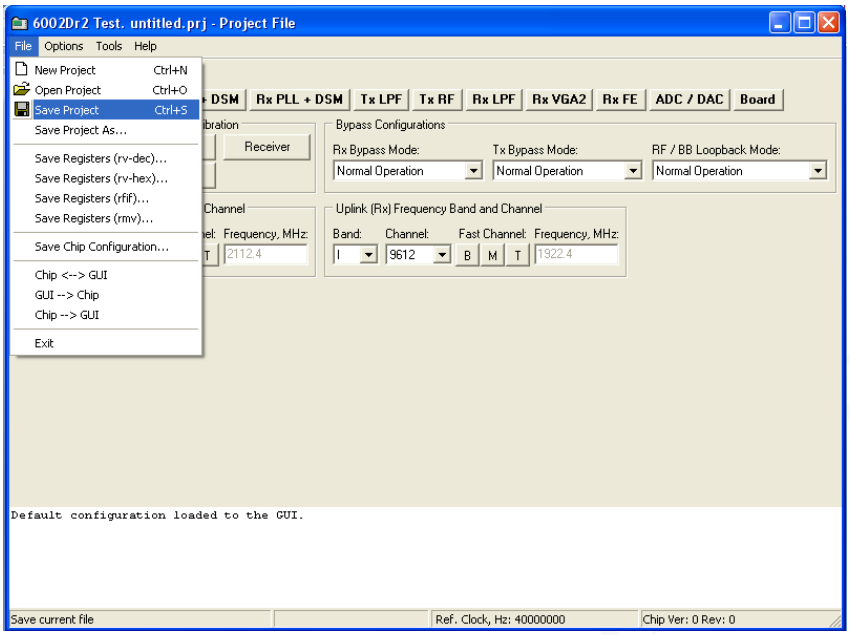

Figure 80 Save Project feature

7.2 Loading *.prj Files

A *.prj file can be loaded using the standard windows procedure as shown below.

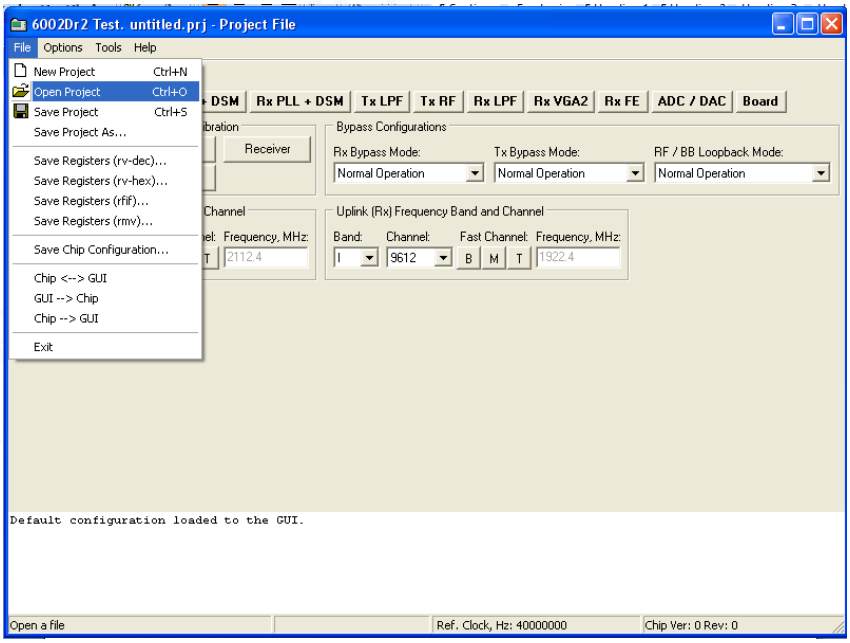

Figure 81 Open project

Select File – Open Project – then select the project that was previously saved from the window file box.

When loading files the software GUI tool can be setup to either load variables into the tool, but not download them to the chip or to download the variable into the tool and auto download them.

Auto Download is enabled by the Options menu as shown below.

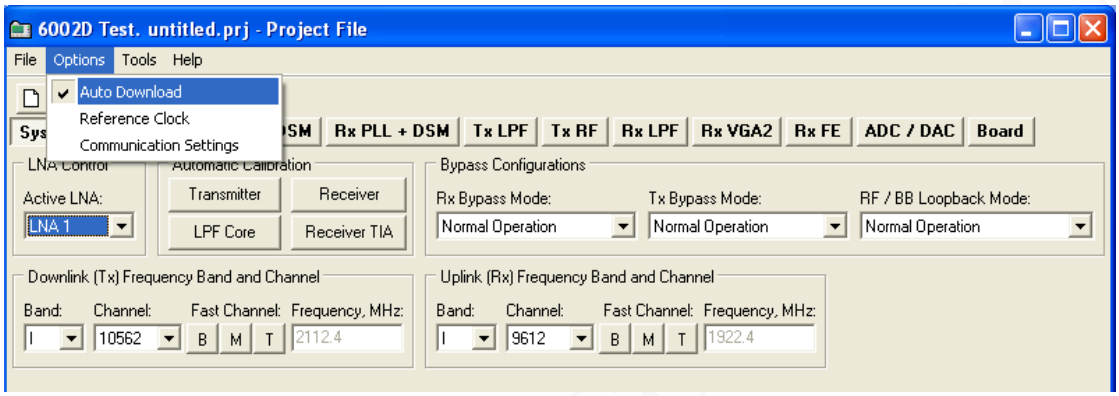

Figure 82 Auto Download feature

If Auto Download is not enabled then the whole SPI map can be sent to the chip by using the download button  as shown below.

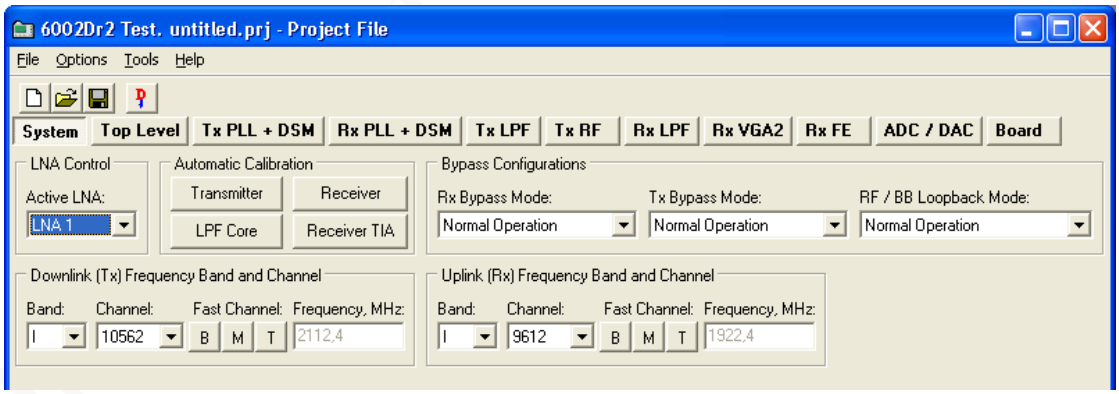

Figure 83 Download Button for Previously Saved Setup

Note : The Ref clock frequency is not strictly part of the SPI information, it is used to calculate the divider ratios for the PLLs. When you start the software for the first time the default clock frequency is 40MHz. You need to change this to the TCXO frequency which typically is 30.72 MHz. If you use a different TCXO frequency you need to change the reference clock (Tools->Reference Clock).

8

Appendix B - Test System Connections

8.1 Basic Setup

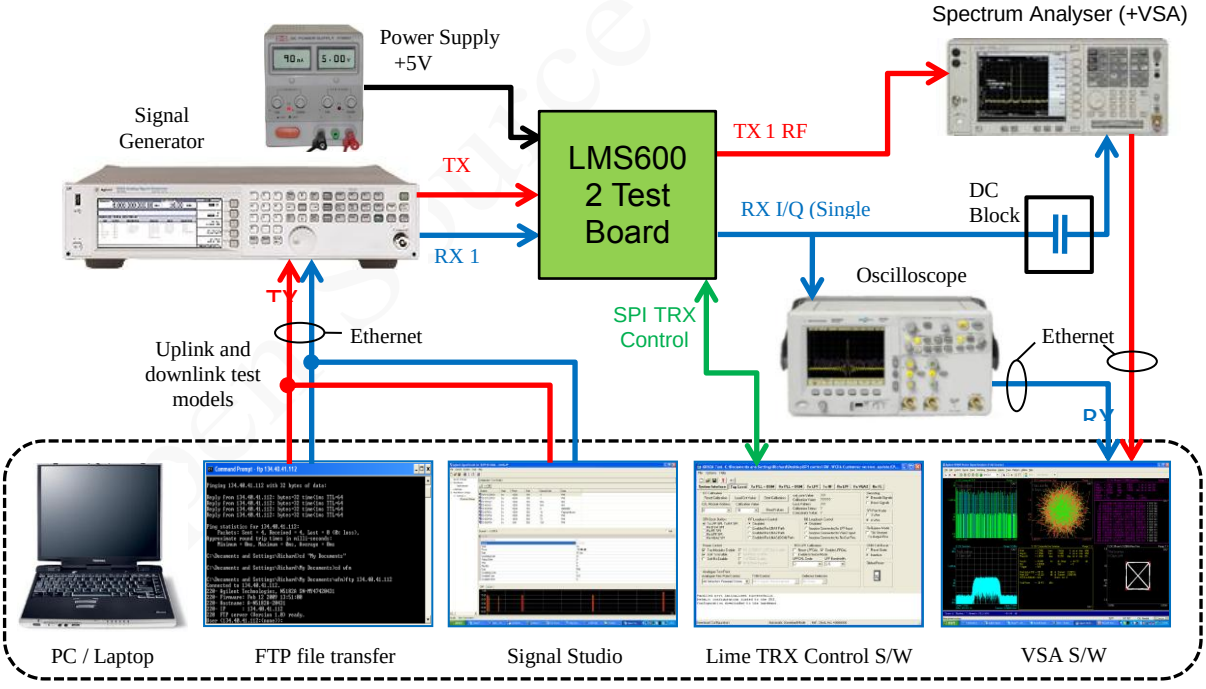

Figure 84 Test system connections for receive and transmit Testing

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8.2 Transmitter Test System Connections

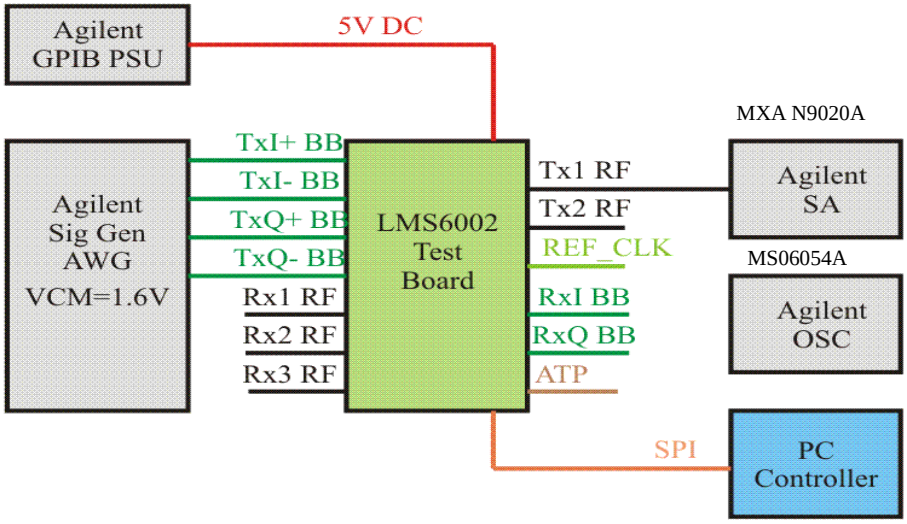

Figure 85 Transmitter test setup

8.3 Receive Test System Connections

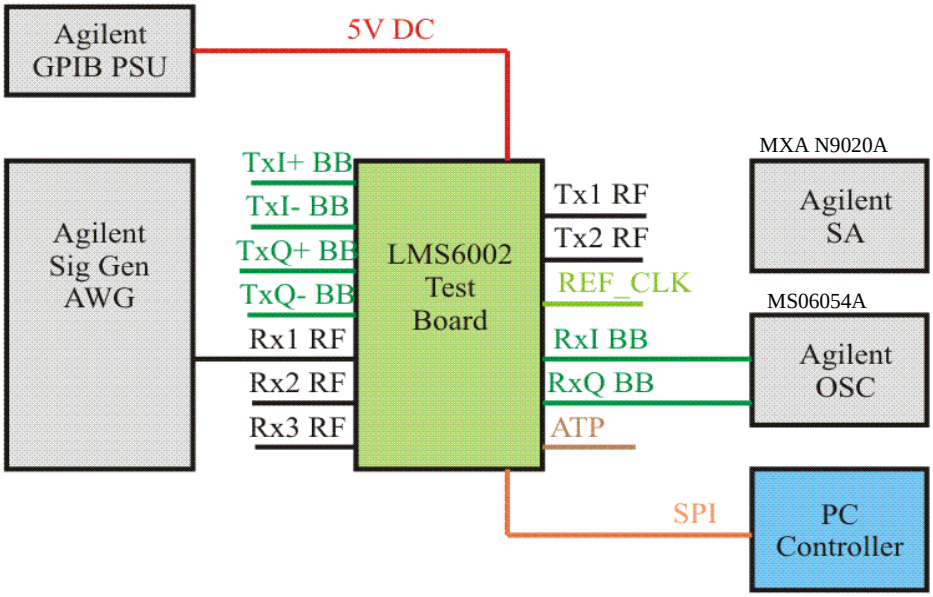

Figure 86 Receiver test setup

9

Appendix C – Signal Generator Setup

This manual uses the Agilent N5182A MXG signal generator with an arbitrary waveform generator and the differential I/Q outputs option (1EL). Other signal generators can be used. However, some issues may arise if the options available for IQ amplitude and phase manipulation which come with the MXG are not supported.

9.1 Agilent MXG Setup

The front panel of the MXG is as follows:

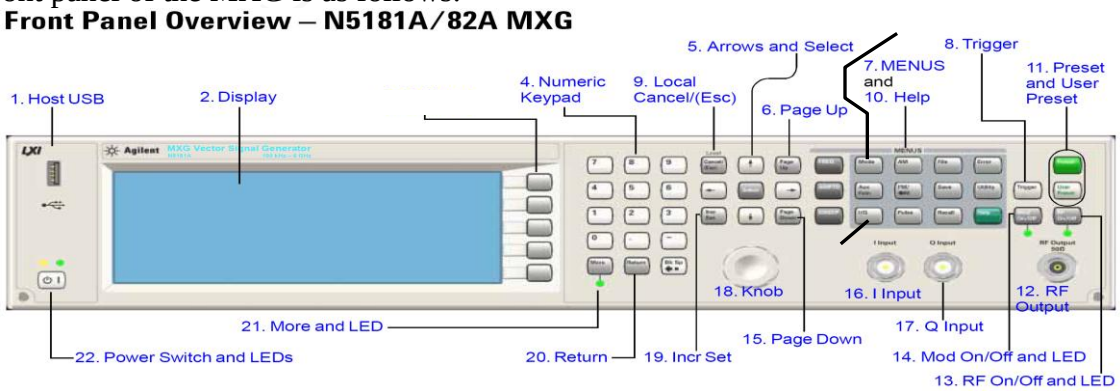

Figure 87 Agilent N5181A/82A MXG Front Panel

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Step 1 – Apply 0.6V common mode offset on IQ outputs

LMS6002D Analogue inputs require a 0.6V common mode offset voltage with a 300 mVp-p voltage swing for optimum performance.

To apply common m ode offset voltage:

1. Press 'IQ' button (24)
2. Press 'IQ offsets (on/off)' softkey (3. softkey 4)
3. Press 'external output adjustments' softkey (3. softkey 4)
4. Press 'Common Mode I/Q offset' softkey (3. softkey 2)
5. type 0.6 on number pad (4), press 'V' softkey (3. softkey 1)
6. 0.6V should appear on the display next to the 'Common Mode I/Q offset' softkey
7. Press return
    i. Check text next to 'I/Q Adjustments' softkey (3. softkey 1) highlights 'off/on'
    ii. If not press 'I/Q Adjustments' softkey (3. softkey 1), highlighted section should alternate between on and off when pressed.
    iii. press return
    iv. Check text next to 'I/Q' softkey (3. softkey 1) highlights 'off/on'
    v. If not press 'I/Q' softkey (3. softkey 1), highlighted section should alternate between on and off when pressed.

There should now be a 0.6V common mode voltage on the differential IQ connections on the signal generator. This can be verified by measuring the DC level of each of the 4 differential I/Q lines with a multimeter.

Note: Very small DC offset levels in the transmit IQ path can result in LO breakthrough levels changing in the transmit chain. To eliminate or minimize this effect the following practices should be followed:

- IQ cables should be equal length.
- Once I/Q gain and phase calibration is completed, connections should not be modified.
- Cables and connections should not be moved once I/Q gain and phase calibration is completed.

In practice the LMS6002D chip will be soldered to a PCB and connected to a baseband processor so this is purely a test issue.

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Step 2 – Turn on the arbitrary waveform generator

The arbitrary waveform generator will run test vectors which are downloaded to it via either Agilents 'Signal Studio' program or test vectors which can be generated independently via 'Matlab' or C.

Lime has a number of test vector files which are used for test and calibration of the LMS6002D as follows:

- DC.wfm - DC tone for TX CW testing (clock 52MHz).
- onetone1.wfm - single tone at 1MHz offset for sideband suppression calibration/test (clock 52MHz).
- twotone.wfm - two tone signal for linearity testing for MXG and LMS6002D use MXG IQ scaling factor of 30% (clock 52MHz).
- wcdma31.wfm - TM2 WCDMA signal - use MXG IQ scaling factor of 30% (clock=15.36MHz).
- EDGE3.wfm - GSM EDGE modulated test signal - (clock=13MHz).

To download files to the signal generator follow process described in 9.2 section.

To apply the correct file

1. Press 'Mode' button (23)
2. Press 'Dual Arb' softkey (3. softkey 1)
3. Press 'Select waveform' softkey (3. softkey 2)
4. Use up/down arrows (5) or spin knob (18) to select wanted waveform from list.
5. Press 'Select waveform' softkey (3. softkey 1)
6. Name of selected waveform should now be present in display window
7. Soft key list should have moved up one level back to 'Arb'
8. Now change the Arb clock frequency
9. Press 'Arb setup' softkey (3. softkey 3)
10. Press 'Arb sample clock' softkey (3. softkey 1)
11. Type in required frequency on number pad eg for 13MHz type '13' and press 'MHz' softkey (3. softkey 2)
12. Sample clock frequency should now be displayed on the screen.
13. Now scale waveform data if necessary
14. Go to 'Arb' softkey menu
    a. Either press 'return' button from 'Arb setup' menu or
    b. Press 'Mode' button then 'Dual Arb softkey (3. softkey 1)
15. Press 'More' button (21)
16. Press 'Waveform Utilities' softkey (3. softkey 2)
17. Use up/down arrows (5) or spin wheel to highlight wanted waveform from list.
18. Press 'scale waveform data' softkey (3. softkey 2)

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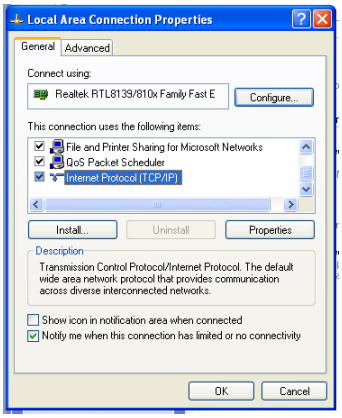
19. Type in required scaling factor e.g.25%, type ’25’ on number pad and press ‘%’ softkey (3. softkey 1).
    Note – even if text next to ‘scaling’ softkey already states 25% (for example) this does not mean it has been applied to the waveform, still follow process.
20. Press ‘Apply to waveform’ softkey (3. softkey 4)
21. Progress bar will show on screen, soft menu will return to level up (Arb utilities).
22. Now return to main ‘Arb’ Menu
    a. Press ‘return’ button twice or
    b. Press ‘Mode’ button then ‘Dual Arb softkey (3. softkey 1)
23. Check Arb in enabled
    a.‘Arb on/off’ softkey (3. softkey 1) text should have on highlighted ‘Off / On’
    b. If not press ‘Arb on/off’ softkey (3. softkey 1) to toggle between on and off.
24. Modulation can be also toggled on and off by the ‘Mod on/off’ button (just above the RF o/p connector). This must also be on – green LED must be illuminated.
    a. Press ‘Mod on/off’ button to toggle modulation on and off.
    Note – Mod on/off button turns modulation on to RF output and IQ output simultaneously. RF does not need to be on for IQ outputs to work

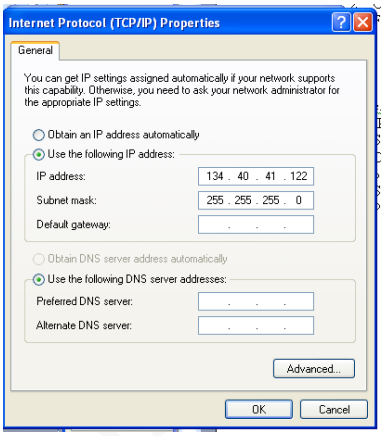
9.2 Downloading *.wfm Files to the Signal Generator

The following process should allow you to download files to the Agilent signal generator. The same process works for MXG and ESG.

This can be done via a network, however these instructions assume a direct connection between a PC running windows XP and the signal generator.

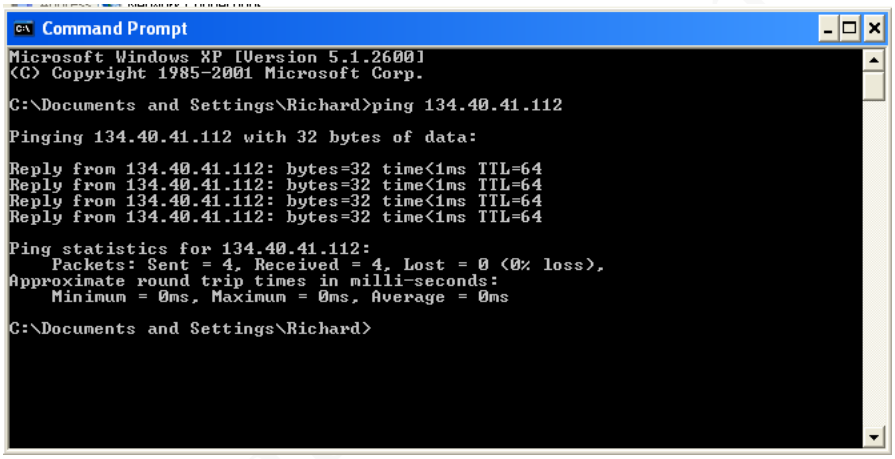
- Connect a cable between PC network port and signal generator LAN port.
- Check LEDs are illuminated on both ends to indicate HW is connected.
- Find IP address of Signal generator
  - Press ‘Utility’ button
  - Press ‘I/O config’ softkey (3. softkey 1)
  - Press ‘LAN setup’ softkey (3. softkey 2)
  - IP address should now be displayed on screen
  - e.g.
    IP Address : 134.40.41.112
    Subnet Mask : 255.255.255.0
- On PC open the ‘Local Area Connection Properties’ box
  - Select Internet Protocol (TCP/IP)
  - Press ‘Properties button
  - Select ‘Use the following IP address’ tick box
  - Set IP address to one close to sig gen, in this case: 134.40.41.122





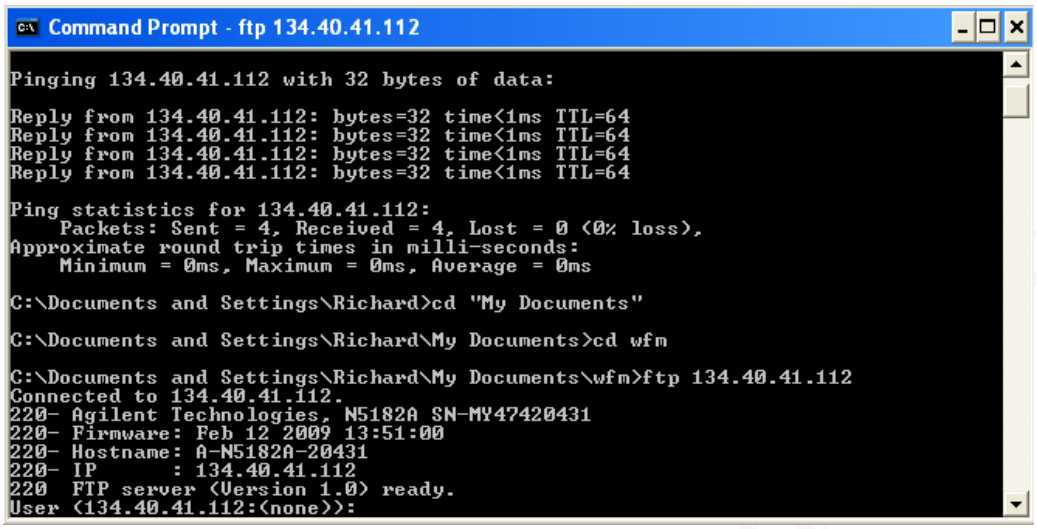
- Set subnet mask to same as sig gen, in this case 255.255.255.0
- Press ok on both open dialog boxes.

- Open a Command Prompt window
  - Start
  - All programs
  - Accessories
  - Command Prompt
- To check connection to signal generator attempt to 'ping' it
  - Type 'ping 134.40.41.112' (or use your sig gen IP address)
- A successful ping result should be returned as shown below.

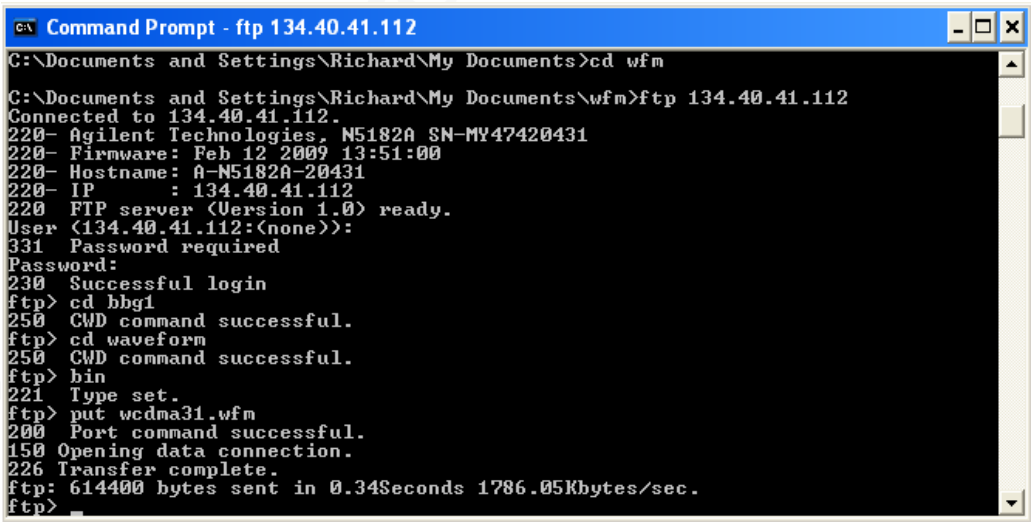


To send wfm files to signal generator the following procedure should be followed.

- Ensure wfm files are in a known directory e.g. 'C:\Documents and Settings\User\My Documents\wfm'.
- In 'Command Prompt' window set directory to the one where the wfm files are located.
- Use FTP to send files to sig gen
- Type 'ftp 134.40.41.112'



- If you are correctly connected the above should be returned.
- Press ‘return’ twice (for user name and password – none needed)
- Type ‘cd bbg1’
- Type ‘cd waveform’
- Type ‘bin’
- Type ‘put wcdma31.wfm’
- Applied command copies files to sig gen – repeat ‘put’ command for all files needed.



- To exit the ftp program type “bye”.
- To close ‘Command Prompt’ window type exit.
- The wfm files should now be visible in the list of Arb files.

10

Appendix D - Common Receiver Test Issues

If there is no baseband signal output from the receiver there are a number of things to check.

10.1 Verify the PLL is locked.

The set up file provided with the test board should have the correct settings so that the synthesizers lock at all available frequencies. This can be verified with a spectrum analyzer by checking to see if the VCO LO leakage signal is on frequency and phase locked. Connect the spectrum analyser to the evaluation board J12 connector. Set receiver input LNA2 and RxPLL for 1950. The VCO leakage signal will be at 2 x LO frequency. Example: Frx=1951MHz the VCO = 2x1951MHz = 3902 MHz.

However if the correct files have been used there is a chance the correct VCO capacitance in the 'RX PLL + DSM' page has not been selected. By observing the scope and changing the VCO capacitance, it is possible to see if this is the problem.

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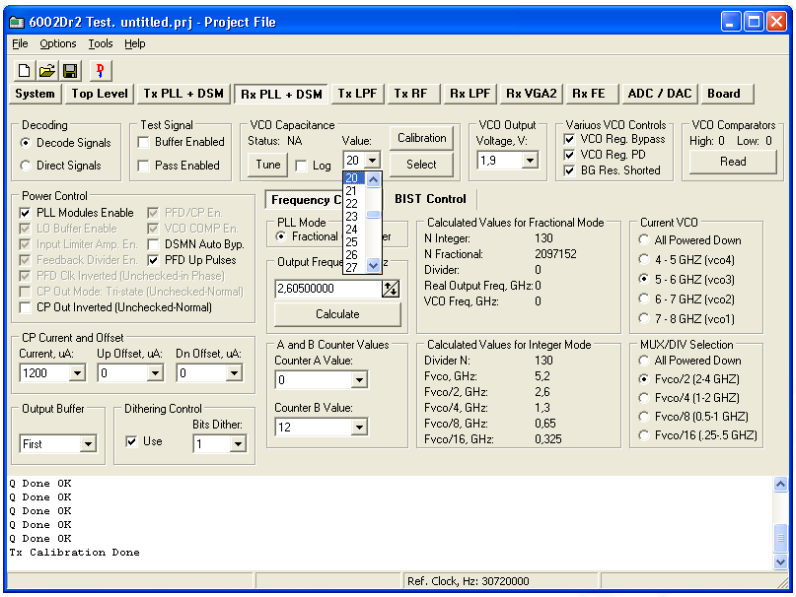

Figure 88 Rx PLL VCO capacitance

By clicking on the number in the VCO capacitance control the drop down box is released, a new number can be selected from this box, or by clicking again in the box the drop down menu will collapse but the box remains highlighted. The up/down arrows on the keyboard can now be used to cycle through the capacitance values. As soon as the number is change it is downloaded to the LMS6002D so scrolling through and observing the effect is quite fast.

There are 3 types of display on the scope that can occur when doing this testing.

1. No receive baseband output as shown below. This implies the synthesizer is not locked so there is no output from the down conversion in the baseband bandwidth.

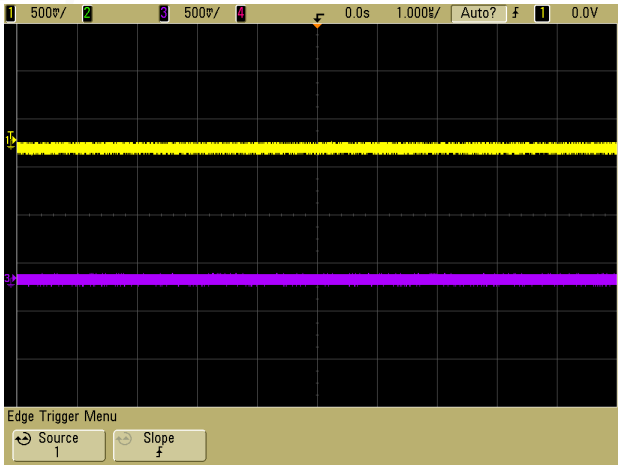

Figure 89 No Receive Baseband Output

2. Non-sinusoidal baseband output as shown below. This occurs when the synthesizer is close to the desired frequency but not locked. This type of behavior usually occurs close to the desired VCO capacitor value.

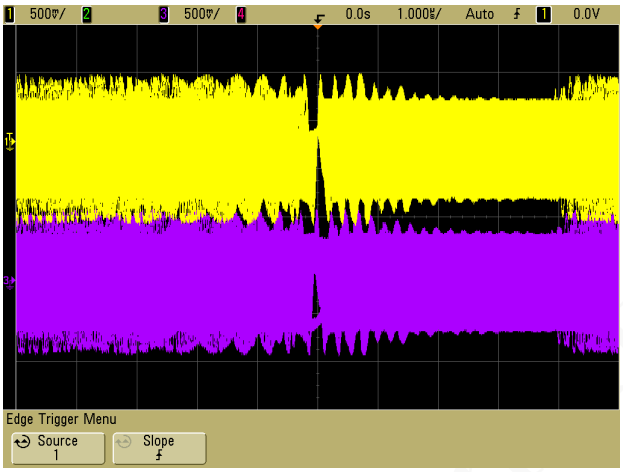

Figure 90 Non-sinusoidal baseband Output

3. Locked PLL. As shown below a sine wave at the difference between the CW RX input frequency and the LO frequency should be observed if the synthesizer locks at the desired in-band frequency and the DC offset is calibrated.

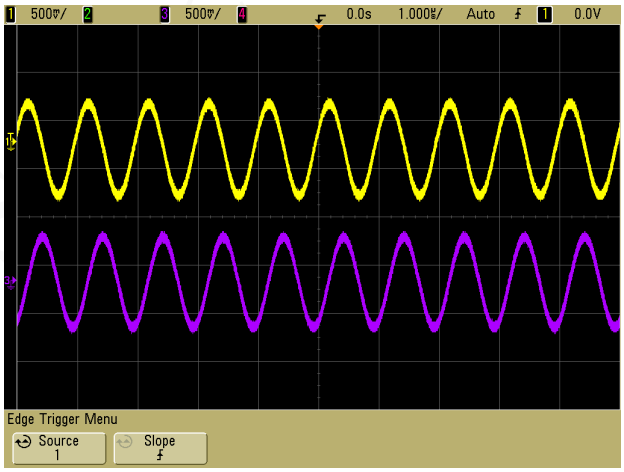

Figure 91 Sinusoidal Baseband Output

There are some ‘rules of thumb’ which may help in the process.

- If all capacitor values are tried and only display A is achieved, it is likely something else is wrong.

- If all capacitor values are tried and display B is achieved with a mid range value, but the synthesiser does not subsequently lock then there may be a problem. Please contact Lime for assistance.

- If display A is achieved but at the end of the capacitor range (0 or 63) then the VCO calibration file will need to be updated.

If the frequency is lowered the cap value goes down, if it is increased the cap value goes up. Usually the PLL locks over a range of cap values, the optimum phase noise performance is usually obtained in the middle of the range.

Please note this is a problem solving procedure and these are rules of thumb but not comprehensive rules. The provided VCO calibration files should set up the synthesiser properly. If assistance is needed please contact Lime so the root problem with the SPI application software can be found.

10.2 Is the Correct LNA Selected

If the lower level pages of the SPI SW are used then there are 2 things which need to be changed to change LNA – the LNA itself on the RX FE page and the output buffer on the RX PLL+ DSM page.

If the control on the 'System interface' page is used both these are changed together and the correct path will be set up.

10.3 Is the Correct Rx VGA 2 Gain Selected

Default gain for RX VGA2 when the software starts is 3, change it to 30 to get a good level output for the scope.